Controlled growth of single-crystal graphene wafers on twin-boundary-free Cu(111) substrates

Yeshu Zhu, Jincan Zhang, Ting Cheng, Jilin Tang, Hongwei Duan, Zhaoning Hu, Jiaxin Shao, Shiwei Wang, Mingyue Wei, Haotian Wu, Ang Li, Sheng Li, Osman Balci, Sachin M. Shinde, Hamideh Ramezani, Luda Wang, Li Lin, Andrea C. Ferrari, Boris I. Yakobson, Hailin Peng*, Kaicheng Jia*, Zhongfan Liu**

Y. Zhu, J. Tang, J. Shao, S. Wang, S. Li, H. Peng, Z. Liu

Center for Nanochemistry,

Beijing Science and Engineering Center for Nanocarbons

Beijing National Laboratory for Molecular Science

College of Chemistry and Molecular Engineering

Peking University

Beijing 100871

P. R. China

E-mail: hlpeng@pku.edu.cn, zfliu@pku.edu.cn

Y. Zhu, J. Tang, H. Duan, J. Shao, S. Li, L. Wang

Academy for Advanced Interdisciplinary Studies
Peking University
Beijing 100871
P. R. China

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Y. Zhu, Z. Hu, J. Shao, S. Wang, M. Wei, A. Li, S. Li, L. Wang, L. Lin, H. Peng, K. Jia, Z. Liu
Technology Innovation Center of Graphene Metrology and Standardization for State Market Regulation, Beijing Graphene Institute
Beijing 100095
P. R. China
E-mail: jiakc@bgi-graphene.com

J. Zhang, O. Balci, S. M. Shinde, H. Ramezani, A. C. Ferrari

Cambridge Graphene Centre

University of Cambridge

Cambridge CB3 0FA

United Kingdom

T. Cheng, B. I. Yakobson

Department of Materials Science & NanoEngineering

Rice University

Houston

Texas 77005

United States

E-mail: biy@rice.edu

H. Duan, L. Wang

National Key Laboratory of Advanced Micro and Nano Manufacture Technology

School of Integrated Circuits

Peking University

Beijing 100871

P. R. China

Z. Hu, H. Wu, L. Lin

School of Materials Science and Engineering

Peking University

Beijing 100871

P. R. China

A. Li

College of Science

China University of Petroleum

Beijing 102249

P. R. China

B. I. Yakobson

Department of Chemistry

Rice University

Houston

Texas 77005

United States

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Abstract

Single-crystal graphene (SCG) wafers are needed to enable mass-electronics and optoelectronics owing to their excellent properties and compatibility with silicon-based technology. Controlled synthesis of high-quality SCG wafers can be done exploiting single-crystal Cu(111) substrates as epitaxial growth substrates recently. However, current Cu(111) films prepared by magnetron sputtering on single-crystal sapphire wafers still suffer from in-plane twin boundaries, which degrade the SCG chemical vapor deposition. Here, we show how to eliminate twin boundaries on Cu and achieve 4'' Cu(111) wafers with ~95% crystallinity. The introduction of a temperature gradient on Cu films with designed texture during annealing drives abnormal grain growth across the whole Cu wafer. In-plane twin boundaries are eliminated via migration of out-of-plane grain boundaries. SCG wafers grown on the resulting single-crystal Cu(111) substrates exhibit improved crystallinity with >97% aligned graphene domains. As-synthesized SCG wafers exhibit an average carrier mobility up to 7284 $cm^2V^{-1}s^{-1}$ at room temperature from 103 devices and a uniform sheet resistance with only 5% deviation in 4'' region.

1. Introduction

The last decade has witnessed great advances in the graphene-based electronics and optoelectronics.[1-8] Owing to its unique properties, graphene is excellent platform for

high-speed photodetectors[9-11] and high-performance sensors.[12,13] In this regard, wafer-scale growth of single-crystal graphene (SCG) is highly required for fulfilling the requirements for real device applications. Chemical vapor deposition (CVD) growth of graphene on single-crystal Cu(111) has become a promising approach to synthesize SCG wafers,[14-17] which can enable the aligned nucleation of graphene domains and subsequent seamless stitching.[18]

The preparation of single-crystal Cu(111) substrates can be down in two ways: (1) mono-crystallization of polycrystalline Cu foils;[19] (2) epitaxial deposition of Cu films on single-crystal templates.[20] Recently, sub-meter-sized single-crystal Cu(111) foils have been achieved by abnormal grain growth,[21] together with control on annealing conditions[22,23] and contact stress.[24] However, as-obtained Cu(111) foils commonly suffer from rough surface,[25,26] originating from the rolling lines (height fluctuation up to sub-μm) of commercially polycrystalline Cu. In contrast, single-crystal Cu(111) films grown on *c*-plane single-crystal sapphires are flat and can be used to synthesize SCG wafers with suppressed structural defects such as grain boundaries (GBs) and wrinkles.[14,16] The resulting wafer-based SCG also exhibits promising transferability compared to the counterpart grown on Cu(111) foils, and is compatible with further microelectronic processing.[27-29]

Since the epitaxy of a 3-fold symmetric Cu(111) film on a 6-fold symmetric underlying sapphire surface has two equivalent configurations rotated by 60°,[30] two possible stacking order (ABC stack and ACB stack) would dominate in the final Cu grains and thus form twin

boundaries (TBs) after the thermal annealing.[31-33] Such misalignment of Cu atoms induces thermal grooves at TBs,[34-36] degrading the subsequent SCG CVD. To eliminate Cu TBs, previous attempts mainly focused on the optimization of experimental parameters, such as sapphire pretreatment conditions,[14,36] Cu deposition temperature,[30,37] and annealing atmosphere[15,31]. However, the resulting single-crystal regions of Cu(111) films are commonly limited to cm scale, and the underlying mechanism of the elimination of TBs remains unclear. Atomic sputtering epitaxy is reported to achieve the fabrication of single-crystal Cu(111) films with the utilization of single-crystal Cu targets and wires.[38] The resulting Cu films exhibit well-organized (111) facet out of plane,[39] but in-plane twin structures still exist.[40] Thus, efforts are still needed to achieve twin-free Cu(111) single-crystal wafers.

Here, we eliminate in-plane TBs by introducing abnormal grain growth in deposited Cu films. Two factors, initial Cu texture and designed temperature gradient, are key to engineer the out-of-plane and in-plane crystallographic orientation of Cu films. By tuning the temperature distribution during the annealing of sputtered Cu films with polycrystalline texture, the abnormal grain growth of Cu starts from the center, then expanding to the Cu wafer edge. In-plane TBs of Cu would migrate along with the migration of out-of-plane GBs, as confirmed by *in situ* optical microscopy (OM) observations and molecular dynamics (MD) simulations. We get 4'' Cu(111) wafers with ~95% crystallinity, as evidenced by OM, low-energy electron diffraction (LEED), X-ray diffraction (XRD), and electron backscatter diffraction (EBSD). SCG wafers grown on the resulting single-crystal Cu(111) substrates exhibit high (>97%)

alignment of graphene domains. Consequently, the average room temperature carrier mobility of as-grown SCG is 7284 $cm^2V^{-1}s^{-1}$ extracted from 103 devices and the sheet resistance is 574 ± 28 Ω sq^{-1} with 5% deviation over a 4'' region.

2. Results and discussion

Figure 1a is a schematic diagram of the fabrication process of single-crystal Cu(111) wafers (See Methods for details). A 500-nm-thick Cu film is deposited on a 4'' single-crystal sapphire substrate using magnetron sputtering. To induce abnormal grain growth of Cu in a controllable manner, which would eliminate the TBs, a temperature gradient is set. A cold-wall CVD system is utilized as the reaction chamber, where thermal energy is concentrated on the graphite susceptor by Joule heating.[41] A graphite cylinder is placed above the middle of the susceptor, leading to a gradient temperature distribution along the radial direction of the Cu/sapphire wafer (Figure S1, Supporting Information).

Figure 1b and c show the simulation of the temperature distribution by finite element method (Figure S2, Supporting Information), which drives the Cu(111) grain formed at the center to expand across the whole wafer. The temperature applied on the Cu/sapphire wafer can be altered by the size of the graphite cylinder (Figure S3 and S4, Supporting Information). Without the temperature gradient, TBs with thermal grooves are observed throughout the entire 4'' Cu wafer annealed in a constant temperature zone (Figure S5 and S6, Supporting Information). Two adjacent Cu grains with 60° in-plane misorientation are found on the both

sides of the twin boundary by high-resolution (scanning) transmission electron microscopy (HR(S)TEM) (Figure S7, Supporting Information). The density of TBs on annealed Cu film significantly decreases under a temperature gradient, where only a few TBs are observed at the edge of the wafer (Figure S8, Supporting Information). After optimization of the annealing conditions (Figure S9 and S10, Supporting Information), a 4'' single-crystal Cu(111) wafer is obtained (Figure 1d). A mirror-smooth surface can be seen, sign of its single-crystalline and uniformity.

The 4" Cu(111) wafer is then divided into 61 regions (1×1 cm^2) for further detailed characterization. OM is used to distinguish the single-crystal and twin-crystal regions, as identified by the presence of thermal grooves. **Figure 2**a plots the statistics of regions probed by OM images with representative results for single-crystal and twin-crystal regions. The examination of all the 61 regions only yields 3 twin-crystal regions, showing ~ 95% crystallinity of the resulting 4'' Cu(111) wafer (Figure S11 and S12, Supporting Information). In order to evaluate the crystallographic orientation, XRD and EBSD measurements are conducted on 9 regions (Figure S14, Supporting Information). XRD patterns demonstrate a typical Cu(111) peak in θ-2θ scans, and diffraction peaks with 120° periodical intervals in φ scans, indicating (111) orientation out of plane,[39] and excluding in-plane twin structures[31] (Figure 2b and c, and Figure S14, Supporting Information). The uniform color of inverse pole figure (IPF) maps in normal, rolling and transverse direction (ND, RD and TD) verifies the presence of single-crystal Cu(111) without in-plane twin structures (Figure 2d-g, and Figure

S15-17, Supporting Information). 3 evenly distributed points in (001) pole figure (PF) characterization (Figure S18, Supporting Information), are consistent with the 3-fold symmetry of Cu(111).[22] The small misorientation (<1°) of kernel average misorientation (KAM) angles, defined as the average misorientation angle between a central grid and its neighboring grids,[42] also supports the uniform distribution of Cu grain orientation (Figure S19, Supporting Information). LEED characterization is then performed to identify the lattice orientation across a larger area. The LEED patterns acquired from 6 randomly selected regions do not show noticeable changes, consistent with a single out-of-plane orientation of the entire Cu region (Figure S20, Supporting Information).

Atomic force microscopy (AFM) is then used to probe surface morphology. The average surface roughness is 0.36 nm in nine 100 μm^2 regions (Figure S21 and S22, Supporting Information). Slip lines with 60° included angle are observed in Figure S21, consistent with previous observation of the Cu(111) textures.[43] Thermal grooves induced by in-plane TBs are detected for Cu films annealed without temperature gradient, Figure S23. The height profile demonstrates that the depth of thermal grooves is ~ 98 nm, increasing the average surface roughness of twined Cu(111) films to ~ 8.12 nm (Figure S23, Supporting Information). To evaluate the surface flatness of Cu wafers over a large scale, white light interferometry (WLI) measurements are conducted with a length of detection increased to 500 μm (Figure S24, Supporting Information). WLI morphology images show the average surface roughness of 0.51 nm, confirming the flat and uniform nature of our Cu(111) wafers.

To investigate the mechanism for elimination of in-plane TBs on Cu(111) wafers, the annealing process is divided into 4 steps according to the temperature variation, i.e., 25, 500, 750, 1000 °C (Figure S25, Supporting Information). EBSD characterization is conducted on Cu samples underwent above-mentioned 4 annealing duration to study the texture evolution during the formation of Cu(111) single crystals. The initial texture of the deposited Cu films is highly dependent on the magnetron sputtering conditions. E.g., Cu film with (111) dominant orientation is obtained with a moderate sputtering power ranging from 100 ~ 200 W, owing to the epitaxial interaction between Cu and sapphire.[44] When the power is increased to 300 ~ 400 W, sputtered Cu atoms with higher energy are produced, contributing to the transformation into a polycrystalline film with random grains and grain boundaries, as shown in Figure S25a. We found that the formation of polycrystal Cu film under high sputtering power is critical to fabricate twin-free Cu(111) wafer. After the annealing of Cu film with (111) dominant orientation formed by lower sputtering power (100 W), the in-plane twinned structures would survive and no abnormal grain growth was observed, although Cu grains with 60° in-plane misorientation tend to grow larger at 500 ^{o}C, as shown in Figure S25b. Because the close-packed Cu(111) grain has the lowest surface energy,[45] the abnormal grain growth might be replaced by the simultaneous growth of excess Cu(111) grains.

The density of Cu(111) grains for abnormal growth is significantly reduced on Cu films with polycrystalline texture, Figure S25a. The cluttered color of IPF map in ND indicates the existence of abundant small polycrystal grains, and the large angular variation (>5°) in KAM

maps also verifies the random distribution of Cu orientations. The structure of the initial Cu film is examined with HR(S)TEM (**Figure 3**a). This confirms the presence of polycrystal grains, which is also supported by the in-plane strain field maps by geometrical phase analysis (GPA) (Figure 3b).[39] In this case, when the temperature reaches a critical value, i.e. 750 °C in our experiment, an abnormal Cu(111) grain is formed and further expands across the whole wafer at the final temperature of 1000 °C. The cross-sectional HR(S)TEM images of as-obtained Cu film also shows a perfect atomic structure from the interior to the interface, and the corresponding strain field maps analyzed by GPA indicate a uniform lattice strain throughout the entire region (Figure 3c,d).

To further investigate the abnormal grain growth of Cu film at 750 °C, *in situ* OM characterization is conducted (Figure S26 and S27, Supporting Vide 1 and 2, Supporting Information). Driven by the temperature gradient, the migration of Cu GBs is observed (Figure 3e, Supporting Video 3). To understand the contribution of thermal gradient conditions to the formation of single-crystal Cu(111) wafers, MD simulations are employed to clarify the migration behavior of out-of-plane GBs and in-plane TBs (Details seen in Figure S28, Supporting Information). The initially unrelaxed structure is shown in Figure 3f, with TBs and GBs marked by red and white, respectively. The Lindemann index, which compares the average atomic displacement to the mean interatomic spacing, is used to measure the disorder.[46] Figure 3g shows that in the heating and annealing stages, TBs and GBs still exist and hardly move (Figure 3g, 0-9 ns), consistent with *in situ* OM (Figure S27, Supporting

Information). After applying a thermal gradient in the *Z* direction, which is the longest dimension in our simulation, GBs migrate along the temperature gradient (Figure 3g, 9-39 ns and Supporting Video 4, Supporting Information). The in-plane TBs tend to migrate synchronously, following the migration of GBs along the same direction. This can be understood based on the general theory of GB diffusion.[47] Under a high temperature of 1300 K, the Cu atoms near defects are pre-melting and mobile, and the thermal gradient acts as a driving force for defects to migrate. Therefore, we propose that the controlled fabrication of single-crystal Cu(111) wafers contains 3 key steps: (1) Cu(111) grains form with low seed density, as controlled by the initial texture of the deposited Cu film; (2) Abnormal growth of Cu(111) grains expands across the whole Cu wafer driven by temperature-gradient annealing; (3) In-plane TBs are eliminated with the migration of out-of-plane GBs, contributing to the final single-crystal Cu(111) wafer.

Figure 4a,b reveal the influence of Cu TBs on SCG growth. According to a statistics of 1093 isolated graphene domains grown on twined Cu substrates, the aligned graphene domains are 74% (Figure S29, Supporting Information). As the misorientation angle of in-plane twinned Cu(111) polycrystals is 60°, the acquired ratio of aligned graphene domains is lower than theoretical prediction,[48] suggesting the existence of other factors degrading the aligned growth. Apart from the predominant 30°-misorientation, which originates from the local minima of the interface energy between graphene edges and Cu(111) steps,[49] graphene domains with other misorientation angles is also high, indicating that the epitaxy behavior of graphene is changed

by Cu thermal grooves. Graphene grown on twin-free Cu(111) has a significantly enhanced orientation, with ~ 97% aligned domains, with the remaining 3% mainly 30°-misoriented (Figure S30 and S31, Supporting Information).

To further explore the growth behavior of graphene domains on twined Cu(111), AFM and EBSD are conducted on the regions near thermal grooves, because misoriented graphene domains are usually formed in these regions. To highlight the orientation of isolated graphene domains on Cu, phase imaging with better contrast is utilized in AFM characterization[43] (Figure S32, Supporting Information). AFM reveals that the TB crystalline morphology has a remarkable impact on the graphene domain alignment (Figure 4c,d). Nearly no misaligned graphene domains are observed on TBs with line-shaped morphology (Figure S33 and S34, Supporting Information). In contrast, we find graphene domains with rotation angles ranged from 0^{o}~30^{o} on TBs with curve-shaped morphology (Figure S35, Supporting Information). EBSD accounts for this (Figure 4e,f). The crystallographic plane of Cu near curve-shaped TBs tends to deviate from (111) orientation, which might result from stress,[50] and the as-formed Cu surface with other crystal facets influences the graphene domain aligned growth (Figure S36, Supporting Information). Sub-twin grains induced by low-angle (<5°) boundaries are observed on annealed Cu(111), also degrading the aligned growth of graphene domains, due to deviation from the Cu(111) crystal structure (Figure S37 and S38, Supporting Information). In comparison, Cu films across line-shaped TBs show negligible deviation in the original (111)

orientation, beneficial to suppress the formation of misaligned angles graphene domains (Figure S39, Supporting Information).

The aligned growth of graphene domains is a key step to further seamlessly merge them into single-crystal graphene films.[51] We thus use our Cu(111) wafers to grow 4'' SCG by CVD. LEED measurements in Figure S40 verify the identical crystalline orientation of graphene domains. The presence of one set of LEED patterns confirms the single-crystalline nature of the SCG wafer. Selected area electron diffraction (SAED) is then performed on suspended graphene films, transferred on 3-mm-sized TEM grids by a polymer-free method (Figure S41, Supporting Information).[52] The orientation statistics of 60 SAED patterns reveals the single-crystal nature of the probed graphene with similar SAED patterns and rotation angles ($\pm 1.4^{o}$). Raman characterization confirms the crystallinity and uniformity of SLG on Cu(111) (Details seen in the Figure S42a and Table S1, Supporting Information).

SCG wafer is then transferred onto SiO_2/Si via a polymer-assisted wet transfer method.[28] A distribution of sheet resistance $R_s \sim 574 \pm 28\ \Omega\ sq^{-1}$ with a ~ 5% standard deviation over 4'' region is presented in **Figure 5**a. In contrast, R_s of graphene grown on twined Cu(111) is inhomogeneous with standard deviation ~ 16% ($674 \pm 111\ \Omega\ sq^{-1}$) (Figure S43, Supporting Information). The optical transmittance of graphene transferred onto 4'' quartz is ~97.64 ± 0.06% at 550 nm (Figure S44, Supporting Information).

To evaluate the SCG quality, we fabricate 6 batches of devices for mobility measurement. To exclude the impact of contact resistance when evaluating carrier mobility, we perform 4-terminal transport measurement.[10,53] We prepare Hall bar (HB) devices using laser writing, thermal evaporator, and reactive ion etcher (See Methods for details). The channel length (L) and width (W) of the devices are 15 and 10 μm. Raman characterization and analysis is performed after device fabrication to quantify doping and defect density (Figure S42 and Table S1, Supporting Information). OM images of the device arrays and of one device are in Figure 5b and Figure S45. HB devices are measured by sweeping the back gate voltage (V_G) from -30 to 90 V with a fixed source-drain current I_{ds}=50 μA. The voltages of terminals 1 and 2 (right inset in Figure 4b) are recorded to calculate their difference values (V_{12}). Figure 5b plots the resistivity ($\rho = (W*V_{12})/(I_{sd}*L)$) of one device as a function of back gate voltage (V_G). The field effect mobility (μ) is extracted using the direct transconductance method as $\mu = (L*(\partial I_{sd}/\partial V_G))/(V_{12}*C*W)$,[54] where $C = 1.21 \times 10^{-4}$ Fm^{-2} is the back gate capacitance, calculated using 3.9 as the dielectric constant of SiO_2.[53,55] The carrier density (n) is calculated as $n = (V_g-V_{CNP})*C/e$, where V_{CNP} is the back gate voltage at the charge neutrality point (CNP).[48] As shown in Figure 5c, the peak mobilities of hole (μ_h) and electron (μ_e) close to the CNP are ~ 9,129 $cm^2V^{-1}s^{-1}$ and 9,478 $cm^2V^{-1}s^{-1}$ at 290 K and ~ 13,050 $cm^2V^{-1}s^{-1}$ and 13,706 $cm^2V^{-1}s^{-1}$ at 10 K.

Figure 5d plots the conductivity (σ) as a function of n. By fitting the linear and plateau regions of σ at the CNP,[56,57] we extract a residual carrier density (n^*) < 2×10^{11} cm^{-2} at both 290 K and

10 K. n^* is a measure of the spatial inhomogeneity of carriers close to the CNP,[55] which arises due to disorder (e.g., local variations in strain,[59] or chemical doping[60]). Lower n^* indicates less disordered, more homogeneous samples. $n^* \leq 10^{11}$ cm^{-2}, typically associated with either suspended[56] or dry encapsulated samples,[57] is also observed in our SCG at 10 K (Figure S46). Figure 5e is a statistics of room-temperature μ of 24 SCG devices on SiO_2/Si measured under a high vacuum. The observed increase in carrier mobility values further indicates the high quality of graphene (Figure S47). Representative transfer curves of 6 devices are in Figure S48. All devices showed mobility $\mu > 5{,}000$ cm^{2}V^{-1}s^{-1}, with highest $\mu_h \sim 19{,}060$ cm^{2}V^{-1}s^{-1} and highest $\mu_e \sim 11{,}603$ cm^{2}V^{-1}s^{-1}. The average μ_h and μ_e are ~ 8,674 (± 3,444) cm^{2}V^{-1}s^{-1} and 7,629 (± 2,555) cm^{2}V^{-1}s^{-1}, comparable to[61,62] or better than[10,63,64] previous single-crystal and polycrystalline graphene on SiO_2/Si. In order to further investigate the intrinsic electrical quality of our SCG, we minimize graphene doping by optimizing the transfer process and using e-beam lithography method to avoid the impact of photoresist residuals. As shown in Figure S49, the room-temperature carrier mobility up to ~ 28,500 cm^{2}V^{-1}s^{-1} has been successfully reached for our SCG on SiO2/Si, which is superior to previously reported results (Table S2, Supporting Information).

To further evaluate uniformity and consistency, we fabricated 6 batches of SCG HB devices by cutting 6 pieces of cm-sized graphene samples from 2 pieces of 4'' SCG wafers. The statistical results of μ_h measured at ~ 290 K under ambient air are in Figure 5f. For these 103 devices, the

average μ_h is 7,248 (± 2,544) $cm^2V^{-1}s^{-1}$. 17 devices have μ > 10,000 $cm^2V^{-1}s^{-1}$, i.e. ~16.5%, and ~85% devices have μ_h > 5,000 $cm^2V^{-1}s^{-1}$.

3. Conclusion

We report the fabrication of 4'' Cu(111) wafers with ~95% crystallinity. Abnormal grain growth of Cu with polycrystalline texture is achieved under temperature gradient annealing, eliminating in-plane TBs with the migration of out-of-plane GBs. The availability of single-crystal Cu(111) wafers enables growth of graphene with improved crystallinity (>97% aligned domains). As-grown 4'' SCG wafers exhibit an average μ_h ~7284 $cm^2V^{-1}s^{-1}$ measured at ~ 290 K and a uniform sheet resistance with ~5% deviation, paving the way for the controlled synthesis of high-quality graphene wafers.

4. Experiment details:

Preparation of single-crystal Cu (111) wafer:

Single-crystal sapphire wafers (4'', *c* plane, 650 μm thickness, HELIOS New Materials Co., Ltd) are used. Before Cu deposition, they are annealed in O_2 (99.999% purity, Tianjin Jinghai County Huanyu Oxygen Co., Ltd.) for 6 h at 1020 ℃ to eliminate lattice defects.[65] Subsequently, a 500-nm-thick Cu film is deposited by magnetron sputtering (100~400 W direct current power, room temperature and 0.5 nm/s deposition rate, QAM-4W, ULVAC). Then, one Cu/sapphire wafer is placed on a graphite cylinder (5 mm in diameter, 1 mm in

height, 99.98% purity, Tokai Carbon Co., Ltd) and heated to 1005 ℃ with 1000 sccm Ar and 500 sccm H_2 at ~ 800 Pa. To increase the crystallinity of the sputtered Cu film, the Cu/sapphire wafer is annealed for 2 h with the same gas flow. Single-crystal Cu(111) wafer is then obtained after cooling to room temperature.

Growth of single-crystal graphene wafers:

400 sccm H_2 and 2 sccm CH_4 are introduced into the chamber to initiate the SCG CVD growth under atmosphere pressure. 4'' SCG wafer is obtained after 70 mins. To evaluate the graphene alignment, the growth time is decreased into the range of 20-40 mins to synthesize isolated graphene domains.

Transfer of graphene wafers:

Polymer-assisted wet transfer method is used to transfer SCG onto SiO_2/Si and quartz.[28] Poly(methyl methacrylate) (PMMA) (950 K A4, Microchem Corp.) is first spin-coated on 4'' SCG. Then, thermal release tape (TRT) (No.3198MS, Nitto Denko company) is laminated onto the supporting polymer to enhance operability during large-scale transfer. Electrochemical bubbling method is then used to delaminate SCG from Cu(111).[28] Thereafter, SCG and the transfer medium are laminated onto the target substrate after rinsing and drying. The SCG wafer on target substrate is obtained after the transfer medium removal using acetone. Suspended SCG on commercial TEM grids (R 2/1, Au, 300 Mesh, Quantifoil) is prepared by

polymer-free transfer.[52] After placing the TEM grid on top of the SLG wafer, a small drop of isopropanol (~5 μL) is applied to attach the thin carbon film on the TEM grid to the SLG. Following the etching of the Cu film using a $Na_2S_2O_8$ solution (~0.5 M) to facilitate separation of SLG from Cu, the SLG/TEM grid is immersed in deionized water for one full day and subsequently air-dried overnight.

For device fabrication, paraffin wax (Sigma-Aldrich 18634) is used as the support layer to transfer SCG from Cu(111)/sapphire to 285 nm SiO_2/Si.[61,62] First, SCG/Cu(111)/sapphire is put into a mixing solution of ethanol/water (volume ratio ~ 1:1) for 10 h at room temperature to obtain a uniform Cu oxide.[27] Subsequently, paraffin wax pallets are heated to melt at ~ 80 ^{o}C on a hotplate and then dropped atop the SCG, also heated at 80 ^{o}C, followed by spinning at 1000 rpm for 1 min on a spin coater and then solidification in a fridge at -4 ^{o}C for 10 h. After, paraffin/SCG is detached from Cu(111) by electrochemical delamination,[28] performed using paraffin/SCG/Cu as cathode, a Pt anode and an aqueous solution of NaOH (0.5 M) as the electrolyte, with a direct-current voltage (2 ~ 3 V). The paraffin/SCG samples are then washed with deionized water for one week and then transferred to 38 ^{o}C deionized water for 2 h, before being scooped up by piranha (H_2SO_4:H_2O_2 = 3:1 in volume ratio) cleaned SiO_2/Si. The samples on the target substrates are first dried for 10 h in air and then baked in oven at 40 ^{o}C for 24 h. Finally, the samples are soaked in chloroform for 2 days at room temperature to remove paraffin.

Characterization:

The crystallinity of Cu(111) and SCG is characterized by OM (Nikon, LV100ND), SEM (FEI Quattro S, acceleration voltage 5 kV), EBSD (AMETEK EDAX DigiView Camera in combination with EDAX's TEAM, 20 kV), XRD (Bruker D8 ADVANCE, with a Cu–Kα radiation, 40 kV and 40 mA), LEED (Advanced 4-grid LEED OCI, beam energy 80-150 eV), and TEM (FEI Tecnai F20, acceleration voltage 200 kV). AFM (Bruker Dimension Icon, with ScanAsyst mode) and white light interferometry (WLI, Nikon, Optical Profiler BW-S501) are used to probe the surface morphology of Cu(111) wafer. A UV-visible near-infrared (UV-VIS-NIR) spectrophotometer (Perkin Elmer Lambda 950) is utilized for transmittance measurements. Additionally, a four-probe system (CDE ResMap 178) is employed to assess the electrical conductivity of graphene wafers, with the probe distance being at the mm scale. Cross-sectional specimens of deposited and annealed Cu films are prepared by focus-ion beam milling (FEI Strata DB 235). A high-resolution (S)TEM (FEI Titan Cubed Themis G2 300, acceleration voltage 300 kV) is utilized for the lattice-scale structural characterizations.

Raman spectra are collected before and after transfer using 100× objective of Renishaw InVia Raman spectrometer, and a 514 nm laser with a power < 0.5 mW to exclude heating effects. 10 Raman spectra are acquired on SCG/Cu(111) and 35 Raman spectra are collected on one SCG channel region ($8 \times 20\ \mu m^2$) after device fabrication.

Device fabrication:

SCG devices are prepared using a laser writer (LW-405B+, Microtech Srl) with photoresist AZ5214 and developer AZ 726 MIF. Au and Cr are deposited using thermal evaporator (MiniLab 60, Moorfield Nanotechnology Ltd) at 1 and 0.4 nm/s, separately under a high vacuum (at least 10^{-6} torr). The SCG channels are patterned using O_2 plasma etching (3 W, 75 sccm, 10^{-5} torr, 30s) (NanoEtch, Moorfield Nanotechnology Ltd).

Electronic measurement:

The as-fabricated SCG HB devices are measured using a Cascade Probe Station and Parameter Analyzer at room temperature in ambient air by sweeping V_G from -30 V to +90V by applying a constant drain current (50 μA or 100 μA). For the measurement under high vacuum (at least 10^{-6} torr), a Lakeshore probe station and parameter analyzer were used to measure the transfer curves at both room temperature ~ 290 K and low temperature ~ 10 K.

Supporting Information

Supporting Information is available in the online version of the paper.

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Author contributions

Y.Z., J.Z., and T.C. contributed equally to this work. Z.L., K.J., H.P., and B.I.Y. supervised the project. K.J. and Y.Z. conceived the experiment. Y.Z., J.S., S.W., M.W., A.L., S.L. conducted the preparation of single-crystal Cu(111) wafers and CVD growth of graphene wafers. J.Z., O.B., S.M.S., H.R. and A.C.F. took Raman characterization and analysis, device fabrication and electronic measurements. T.J. and Y.Z. conducted the *in situ* OM characterization of grain boundary migration. Y.Z., K.J., J.S., S.W. and M.W. took and analyzed the OM, SEM, EBSD, XRD, LEED, TEM, AFM, WLI, UV-VIS-NIR spectrophotometer results and four-probe system measurement. T.C. conducted MD calculations. D.H. and L.W. conducted and analyzed finite element analysis simulation. Z.H., H.W., and L.L. conducted the transfer of graphene. All authors discussed the results and commented on the manuscript. K.J., Y.Z. and J.Z. wrote the manuscript.

Conflict of interest

The authors declare no conflict of interest.

Data availability

The data that support the findings of this study are available within the article and its Supplementary Information files. Further information is also available from the corresponding author on reasonable request.

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Figure captions

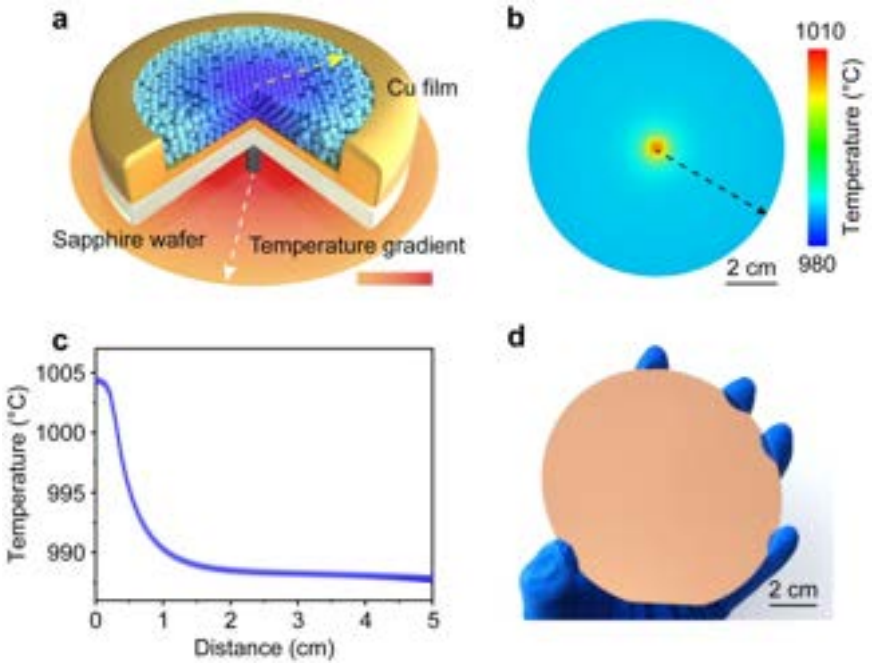

Figure 1. Fabrication of 4'' single-crystal Cu(111) wafer. a, Schematic of formation of single-crystal Cu(111) via abnormal grain growth. **b**, Simulation of temperature gradient applied to 4'' Cu/sapphire wafer using graphene cylinder. **c,** Corresponding temperature profile against the distance from the center of 4'' wafer. **d,** Photograph of as-fabricated 4'' single-crystal Cu(111) wafer.

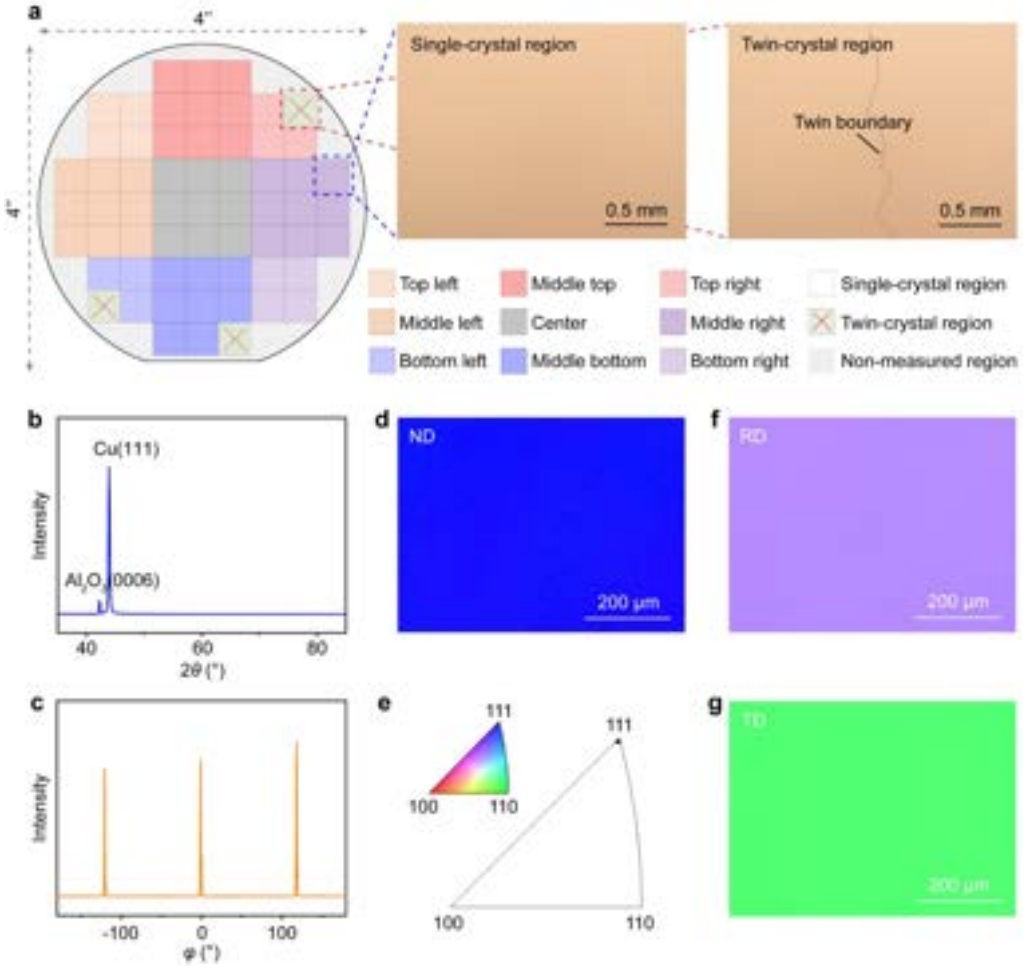

Figure 2. Crystallinity of the resulting 4'' Cu(111) wafer. a, Statistics of crystallinity of 4" Cu(111) wafer. **b,c** XRD (b) θ-2θ scan and (c) φ scan patterns of single-crystal Cu(111) wafer. **d,e** EBSD (d) color maps and (e) corresponding IPF in ND. **f,g** EBSD color maps in (f) RD and (g) TD, respectively.

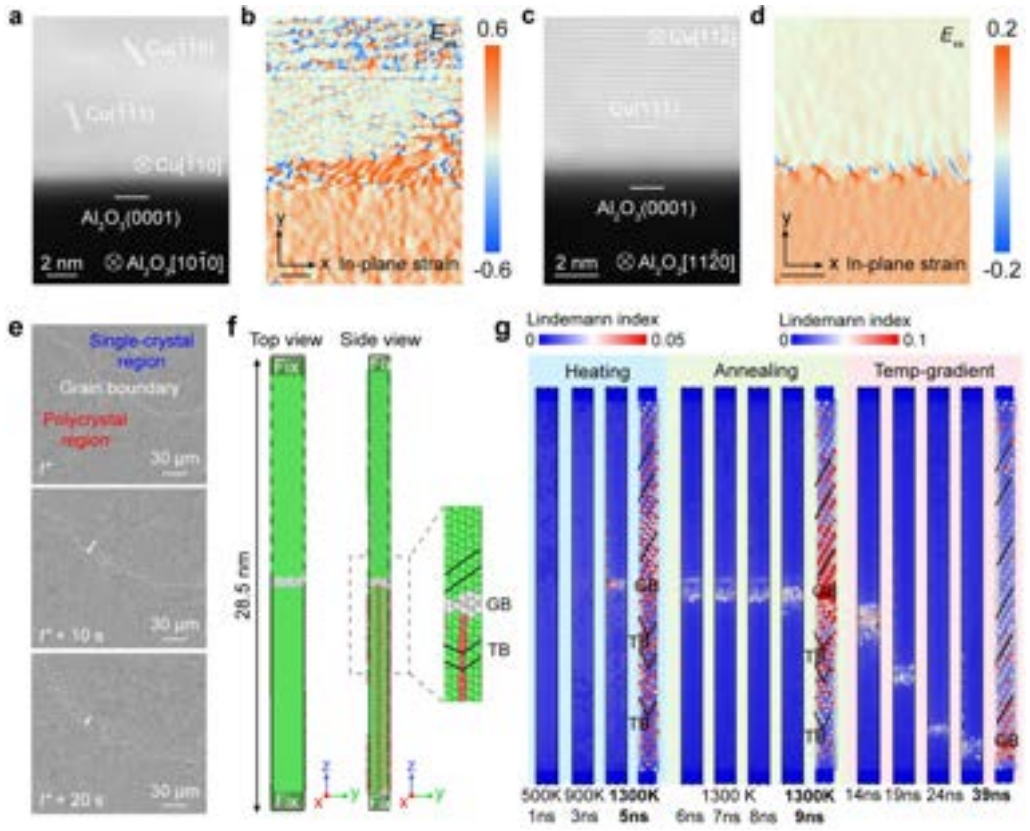

Figure 3. Mechanism for the elimination of in-plane TBs. a, Cross-sectional HR(S)TEM image of the interface between the deposited Cu and Al_2O_3. **b**, In-plane (E_{xx}) strain field maps of (a) by GPA. Scale bar: 2 nm. **c**, Cross-sectional HR(S)TEM image of the interface between the single-crystal Cu(111) and Al_2O_3. **d**, E_{xx} strain field maps of (c) by GPA. Scale bar: 2 nm. **e**, *In situ* OM images of GB migration during abnormal grain growth at 750 ℃. **f**, Top and side views of MD simulation model for the deposited Cu film. TBs and GBs are marked by red and white, respectively, while face-centered cubic domains are in green. The atoms at two ends (shaded box, each ~ 8 Å thick) along the *Z* direction are fixed. **g**, Atomic Lindemann index map during MD simulations in 3 stages: heating (~5 ns), annealing (~4 ns), and with temperature-gradient (~30 ns). At the end of each stage, the side view is shown, and surface atoms are highlighted to show the stacking arrangement.

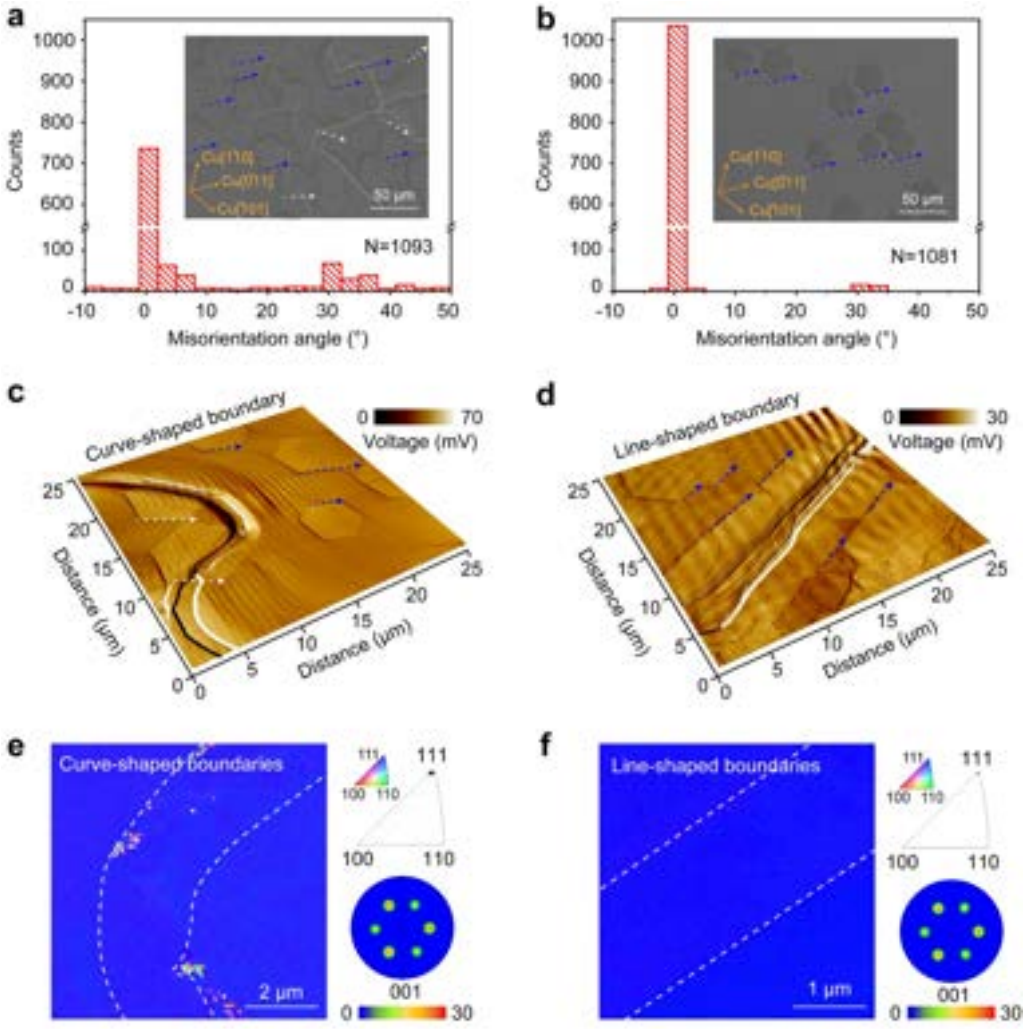

Figure 4. TB influence on graphene orientation. **a,b**, Histograms of graphene domain orientation grown on Cu(111) (a) with and (b) without TBs. Inset: Representative SEM images of as-grown isolated graphene domains. Blue and white dotted arrows denote the orientation of aligned and misaligned graphene domains, respectively. **c,d**, AFM phase images of isolated graphene domains grown on (c) curve-shaped and (d) line-shaped TBs. Blue and white dotted arrows denote the orientation of aligned and misaligned graphene domains, respectively. **e,f**, EBSD characterization results of (e) curve-shaped and (f) line-shaped TBs, respectively.

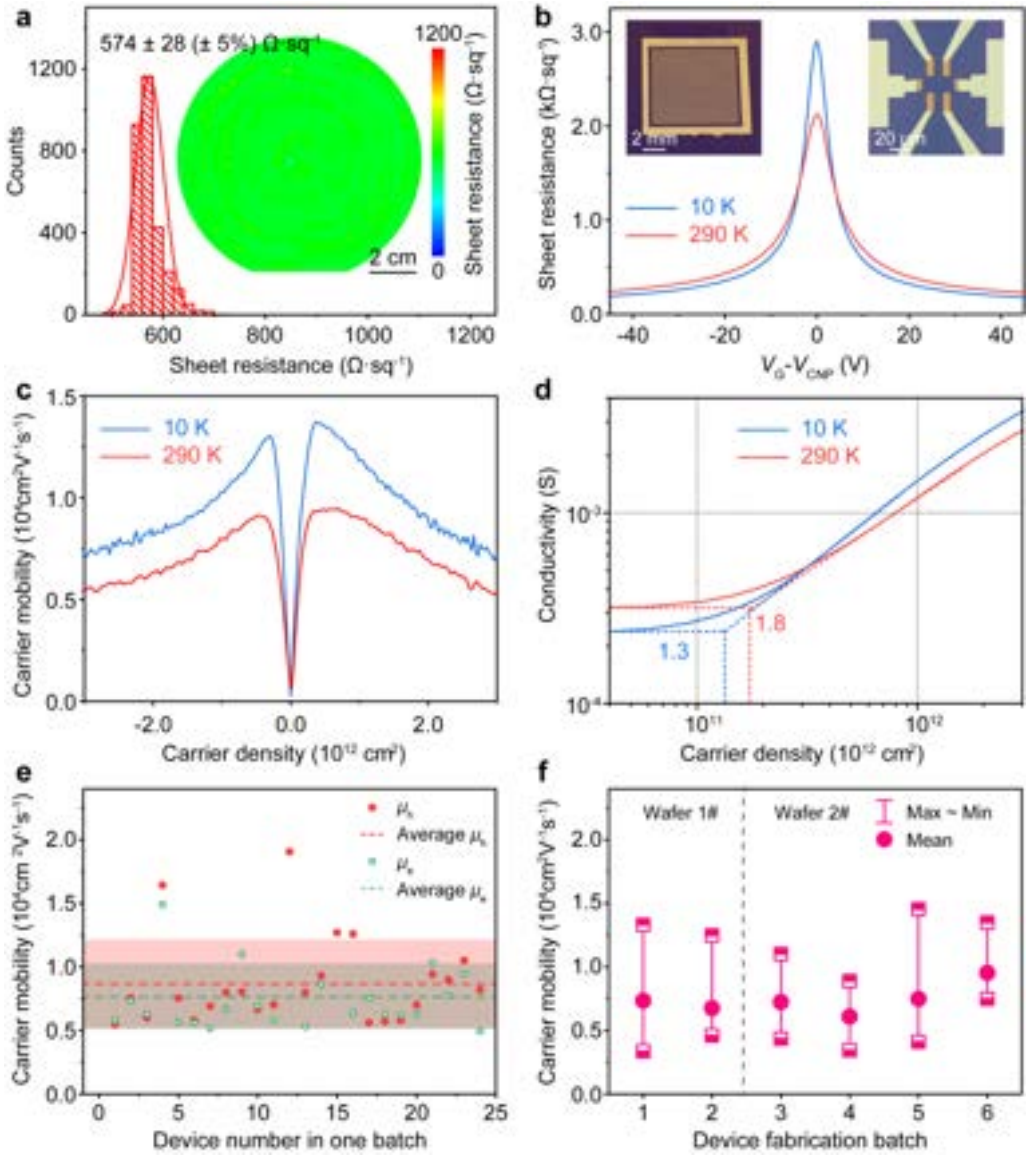

Figure 5. Electronic property of SCG wafer. a, Statistic of R_s of transferred graphene on a 4'' SiO_2/Si. Inset: R_s map. **b**, R_s as a function of the back gate voltage of one device measured at 290 K (red) and 10 K (blue). Inset: OM images of device arrays (left) and one device (right). **c**, Carrier mobility at 290 K (red) and 10 K (blue). **d**, Residual carrier density at 290 K (red) and 10 K (blue). **e**, Statistics of field effect hole (red) and electron (green) mobilities of 24 graphene devices measured at ~290 K under high vacuum (~ 10^{-7} Torr). Dashed lines represent the average μ and shaded areas indicate the standard deviation. **f**, Statistics of μ_h of 6 batches of graphene devices at ~290 K in air.

Yeshu Zhu, Jincan Zhang, Ting Cheng, Jilin Tang, Hongwei Duan, Zhaoning Hu, Jiaxin Shao, Shiwei Wang, Mingyue Wei, Haotian Wu, Ang Li, Sheng Li, Osman Balci, Sachin M. Shinde, Hamideh Ramezani, Luda Wang, Li Lin, Andrea C. Ferrari, Boris I. Yakobson*, Hailin Peng*, Kaicheng Jia*, Zhongfan Liu*

ToC figure

4'' Cu(111) wafers with ~95% crystallinity are achieved with the introduction of a temperature gradient on Cu films with designed texture. During the abnormal growth of Cu(111) grain across the whole Cu wafer, in-plane twin boundaries are eliminated via the migration of out-of-plane grain boundaries. Graphene wafers grown on the resulting Cu(111) substrates exhibit improved crystallinity and electrical properties.