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(54) **PEROVSKITE SEMICONDUCTOR DEVICES**

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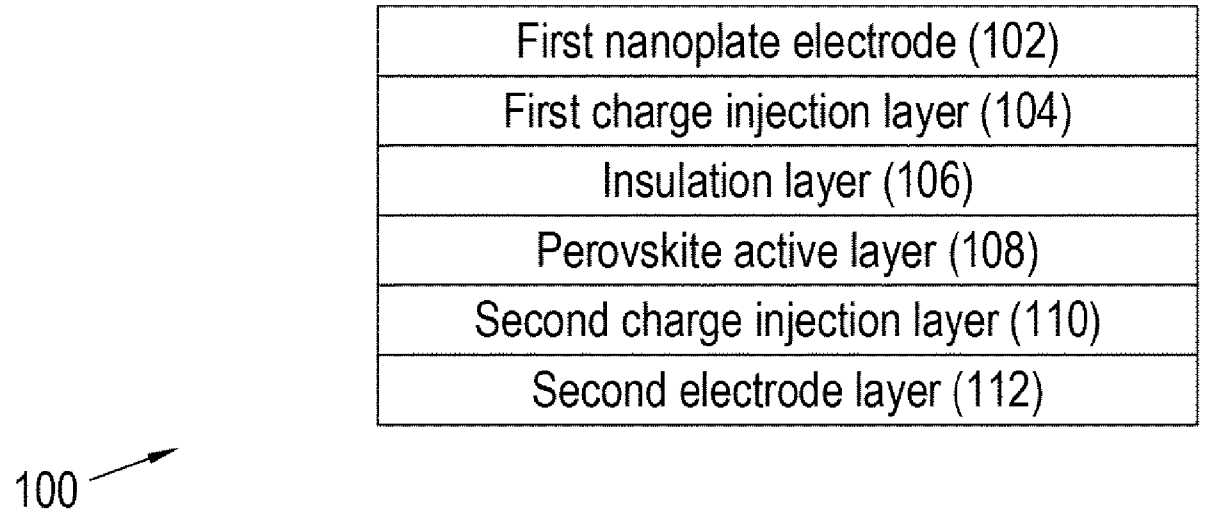
(57) **ABSTRACT**

Semiconductor devices comprising: a semiconductor device comprising: a first electrode comprising conductive material, wherein the conductive material is deposited by ink deposition (for example, layered material inks such as graphene and/or graphite), or wherein the conductive material comprises CVD grown graphene or carbon nanotubes; a first charge transportation layer, wherein the first charge transportation layer is doped with the conductive material of the first electrode; an optional insulation layer; a perovskite active layer; a second charge transportation layer; and a second electrode.



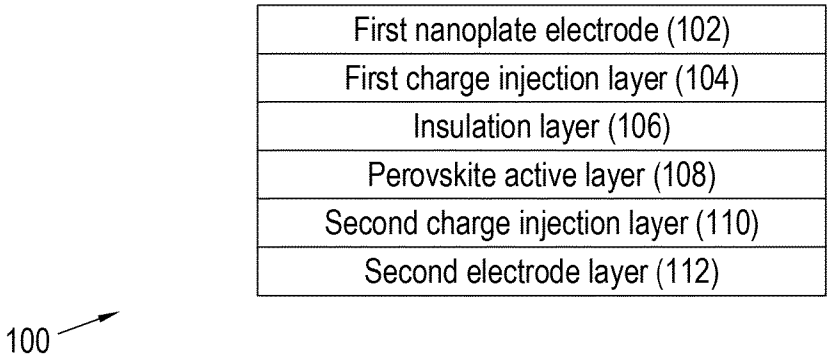

First nanoplate electrode (102)
First charge injection layer (104)
Insulation layer (106)
Perovskite active layer (108)
Second charge injection layer (110)
Second electrode layer (112)
100

Fig. 1

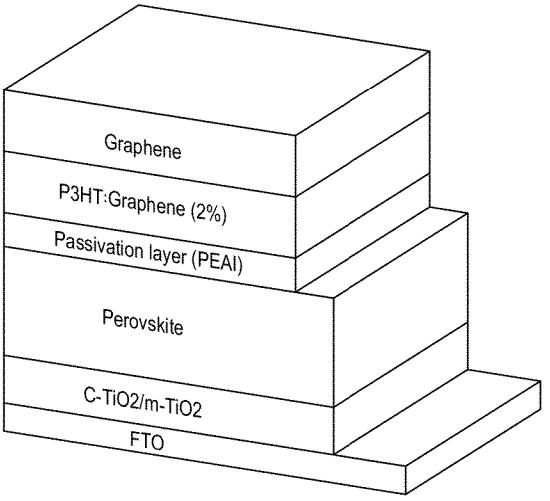

Graphene
P3HT:Graphene (2%)
Passivation layer (PEAI)
Perovskite
C-TiO2/m-TiO2
FTO

Fig. 2

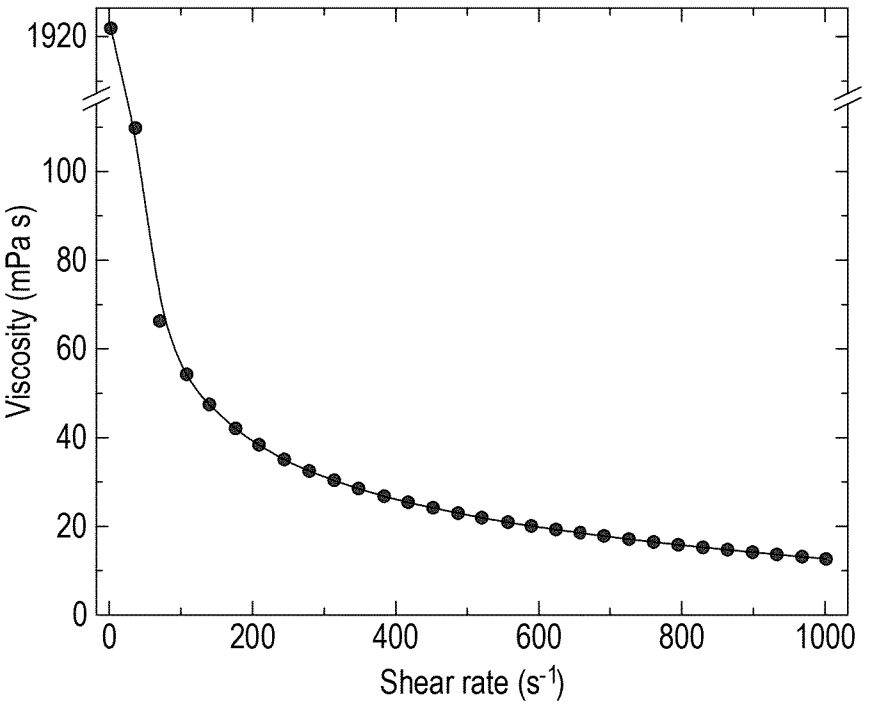

1920
100
80
60
40
20
0
Viscosity (mPa s)
0
200
400
600
800
1000
Shear rate (s-1)

Fig. 3

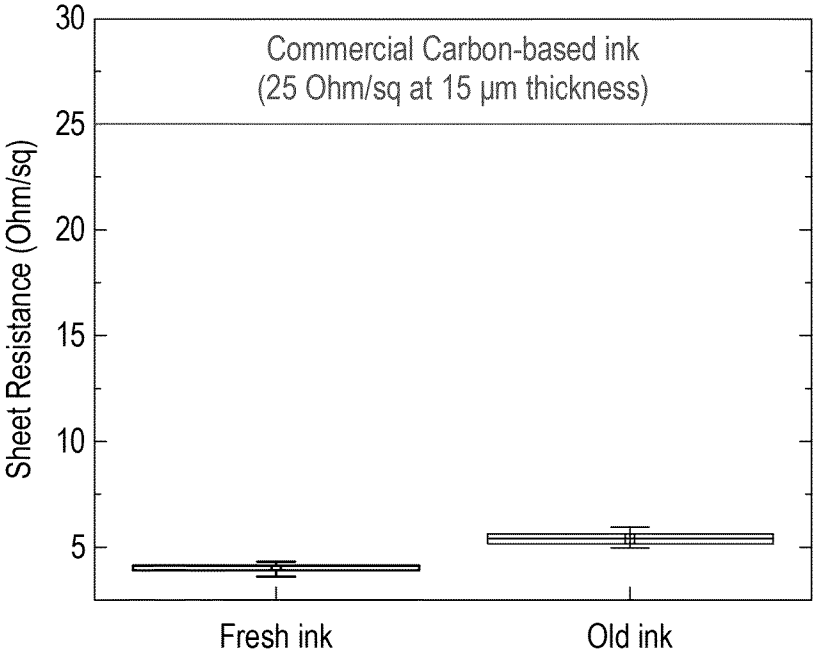

30
25
20
15
10
5
Sheet Resistance (Ohm/sq)
Commercial Carbon-based ink
(25 Ohm/sq at 15 µm thickness)
Fresh ink
Old ink

Fig. 4a

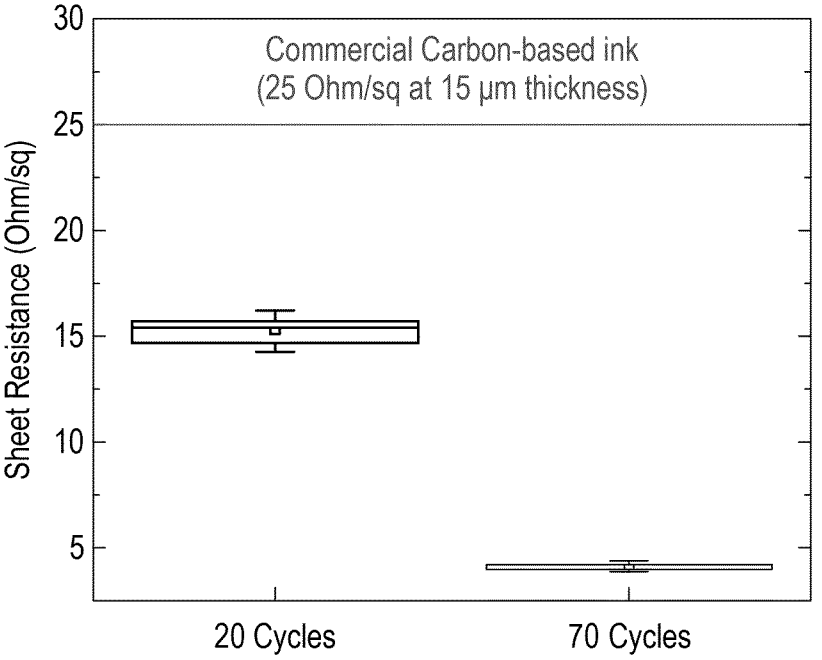

Commercial Carbon-based ink
(25 Ohm/sq at 15 μm thickness)
Sheet Resistance (Ohm/sq)
30
25
20
15
10
5
20 Cycles
70 Cycles

Fig. 4b

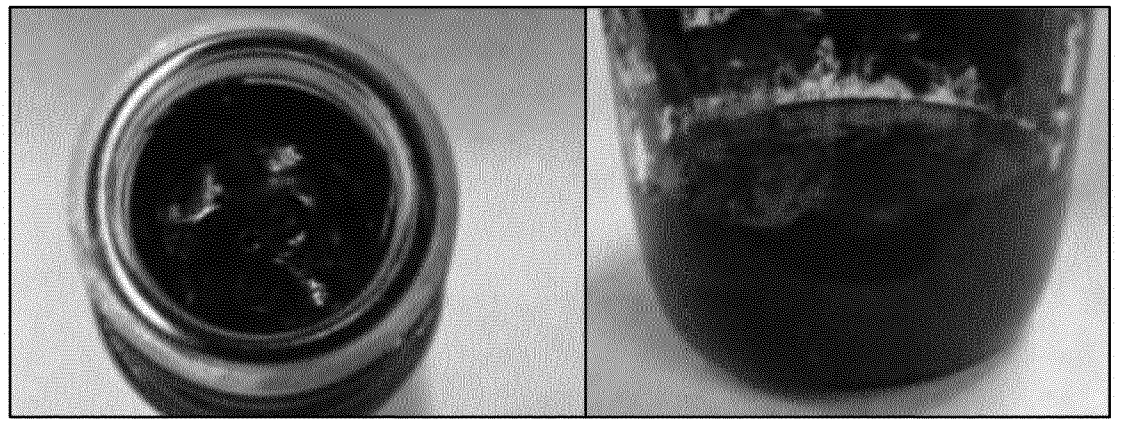


Fig. 5

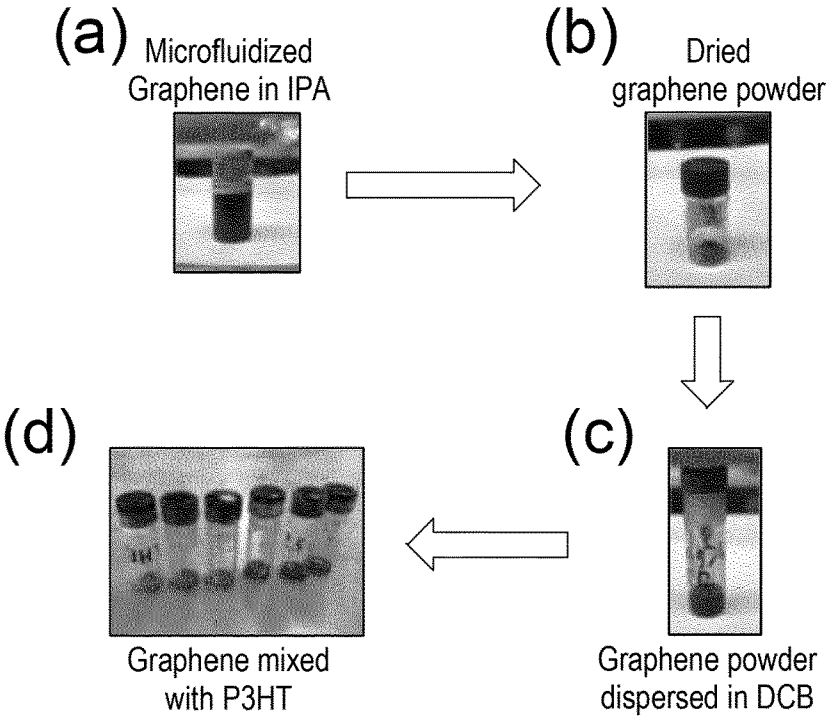

(a)
Microfluidized
Graphene in IPA
(b)
Dried
graphene powder
(c)
Graphene powder
dispersed in DCB
(d)
Graphene mixed
with P3HT

Fig. 6

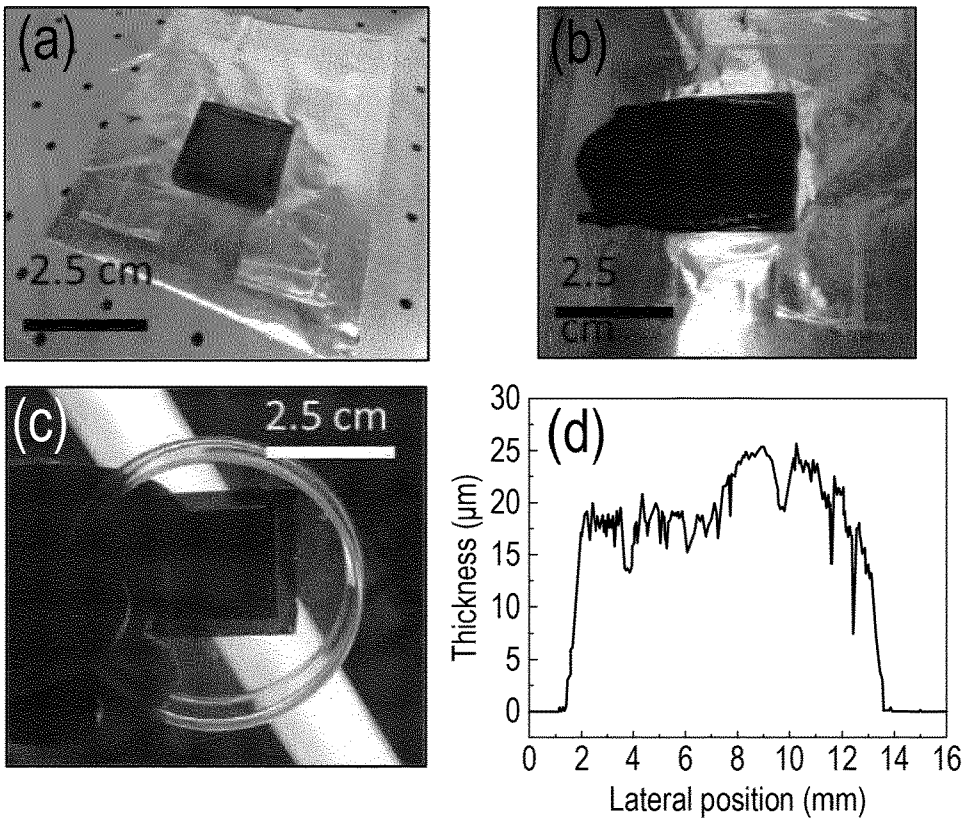

(a)
2.5 cm
(b)
2.5
cm
(c)
2.5 cm
(d)
Thickness (μm)
0
5
10
15
20
25
30
0
2
4
6
8
10
12
14
16
Lateral position (mm)

Fig. 7

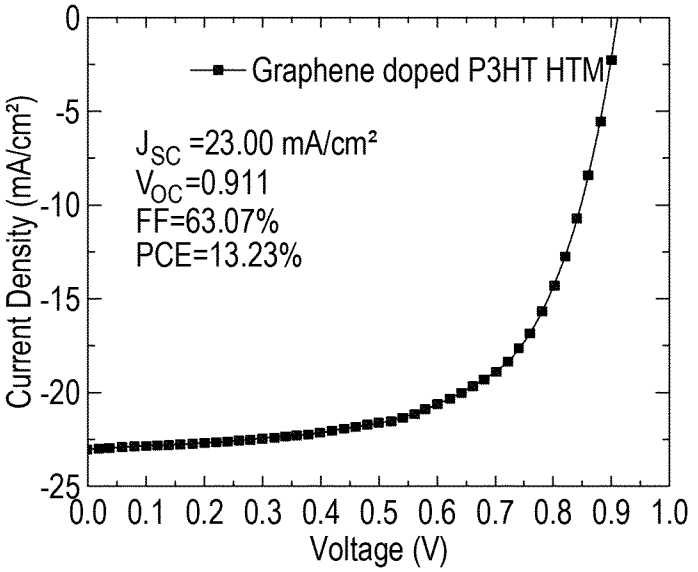

Graphene doped P3HT HTM
J_{SC} =23.00 mA/cm²
V_{OC}=0.911
FF=63.07%
PCE=13.23%
Current Density (mA/cm²)
Voltage (V)
0
-5
-10
-15
-20
-25
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0

Fig. 8

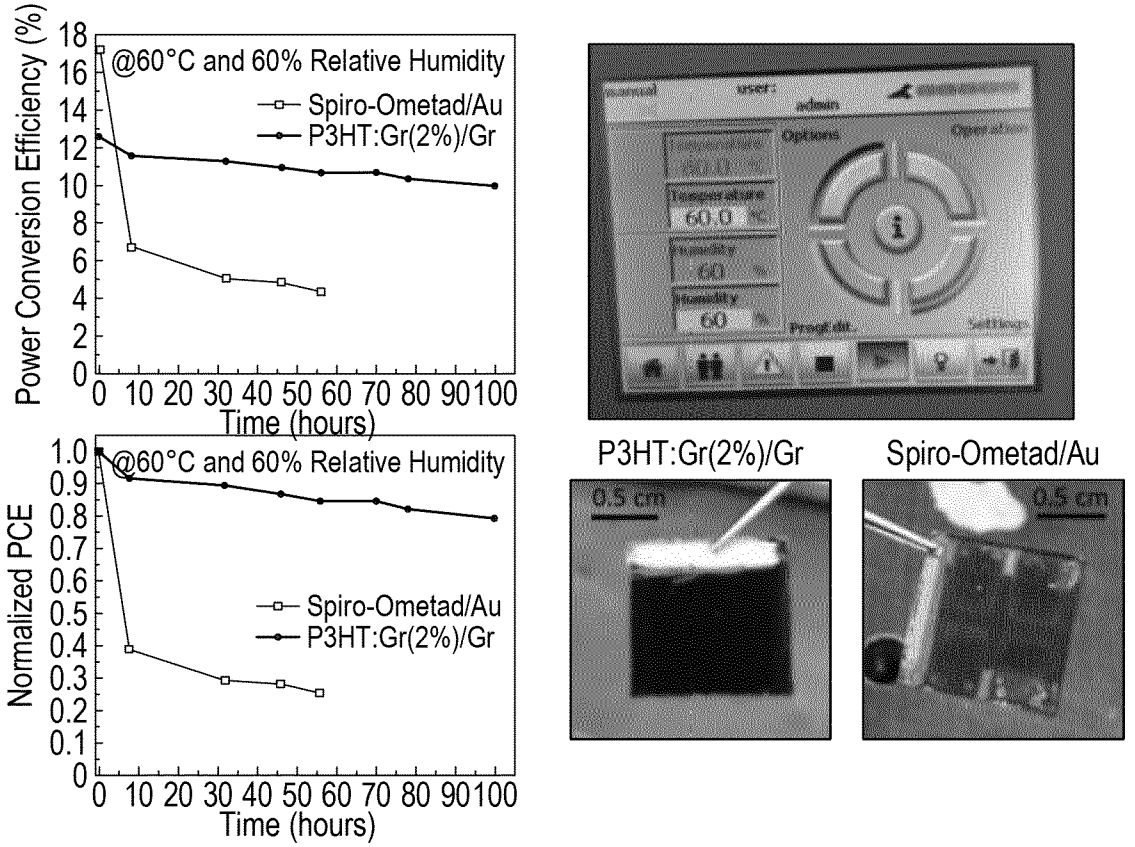

@60°C and 60% Relative Humidity
Spiro-Ometad/Au
P3HT:Gr(2%)/Gr
Power Conversion Efficiency (%)
Time (hours)
@60°C and 60% Relative Humidity
Spiro-Ometad/Au
P3HT:Gr(2%)/Gr
Normalized PCE
Time (hours)
P3HT:Gr(2%)/Gr
Spiro-Ometad/Au
0.5 cm
0.5 cm

Fig. 9

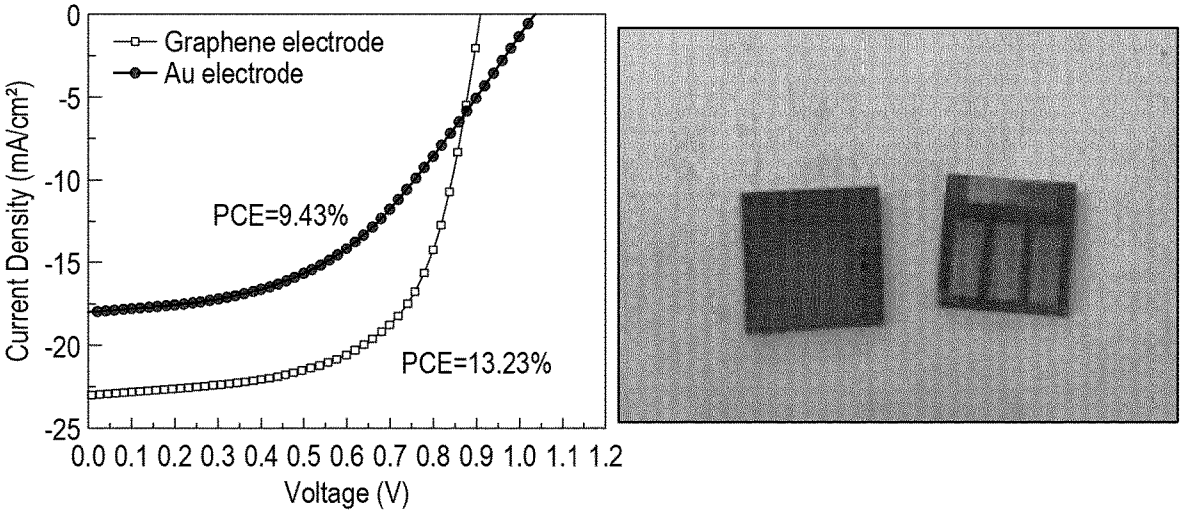

Graphene electrode
Au electrode
PCE=9.43%
PCE=13.23%
Current Density (mA/cm²)
Voltage (V)
0
-5
-10
-15
-20
-25
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2

Fig. 10

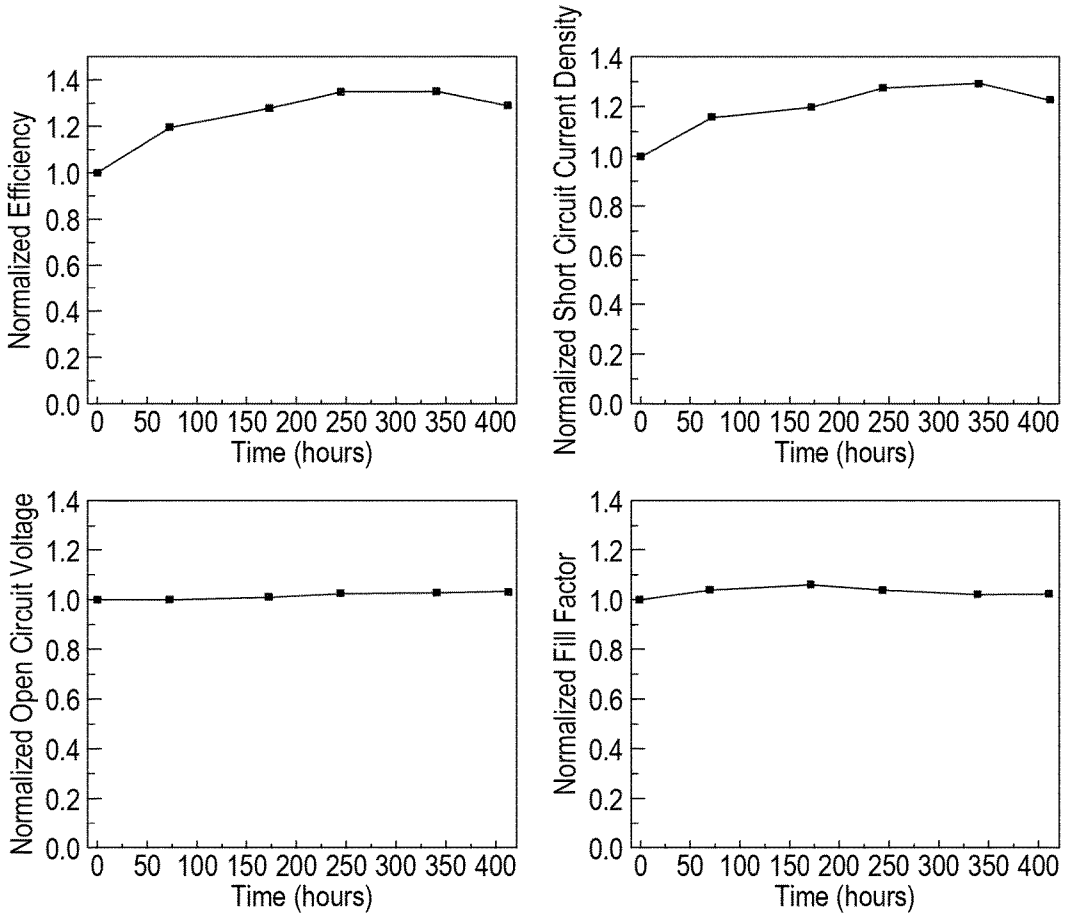

Normalized Efficiency
Normalized Short Circuit Current Density
Normalized Open Circuit Voltage
Normalized Fill Factor
Time (hours)
0 50 100 150 200 250 300 350 400
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4

Fig. 11

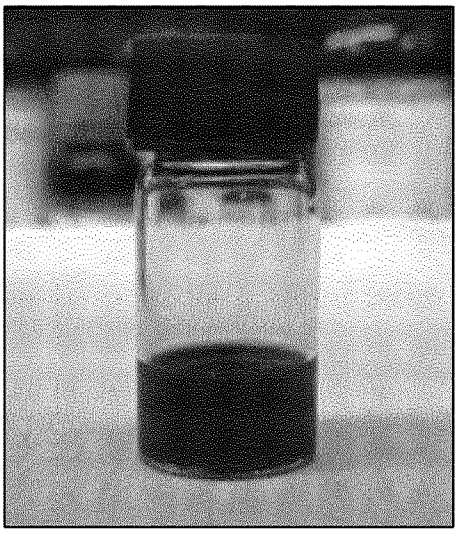
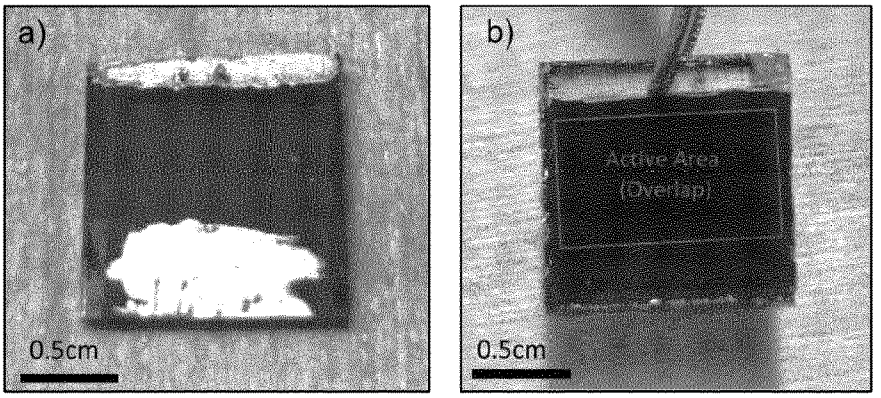


Fig. 12


a)
0.5cm
b)
Active Area
(Overlap)
0.5cm

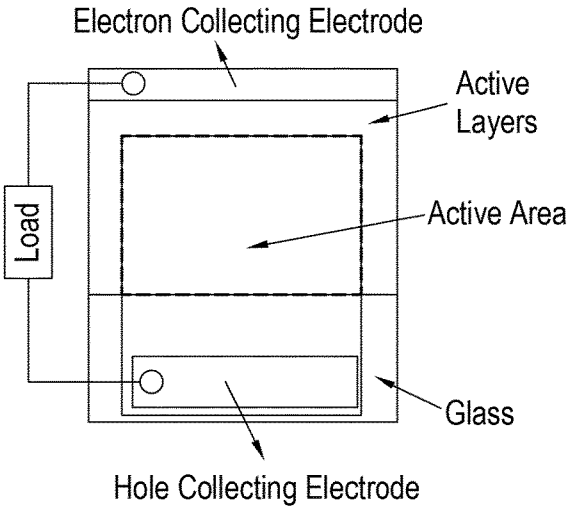

Electron Collecting Electrode
Active
Layers
Load
Active Area
Glass
Hole Collecting Electrode

Fig. 13

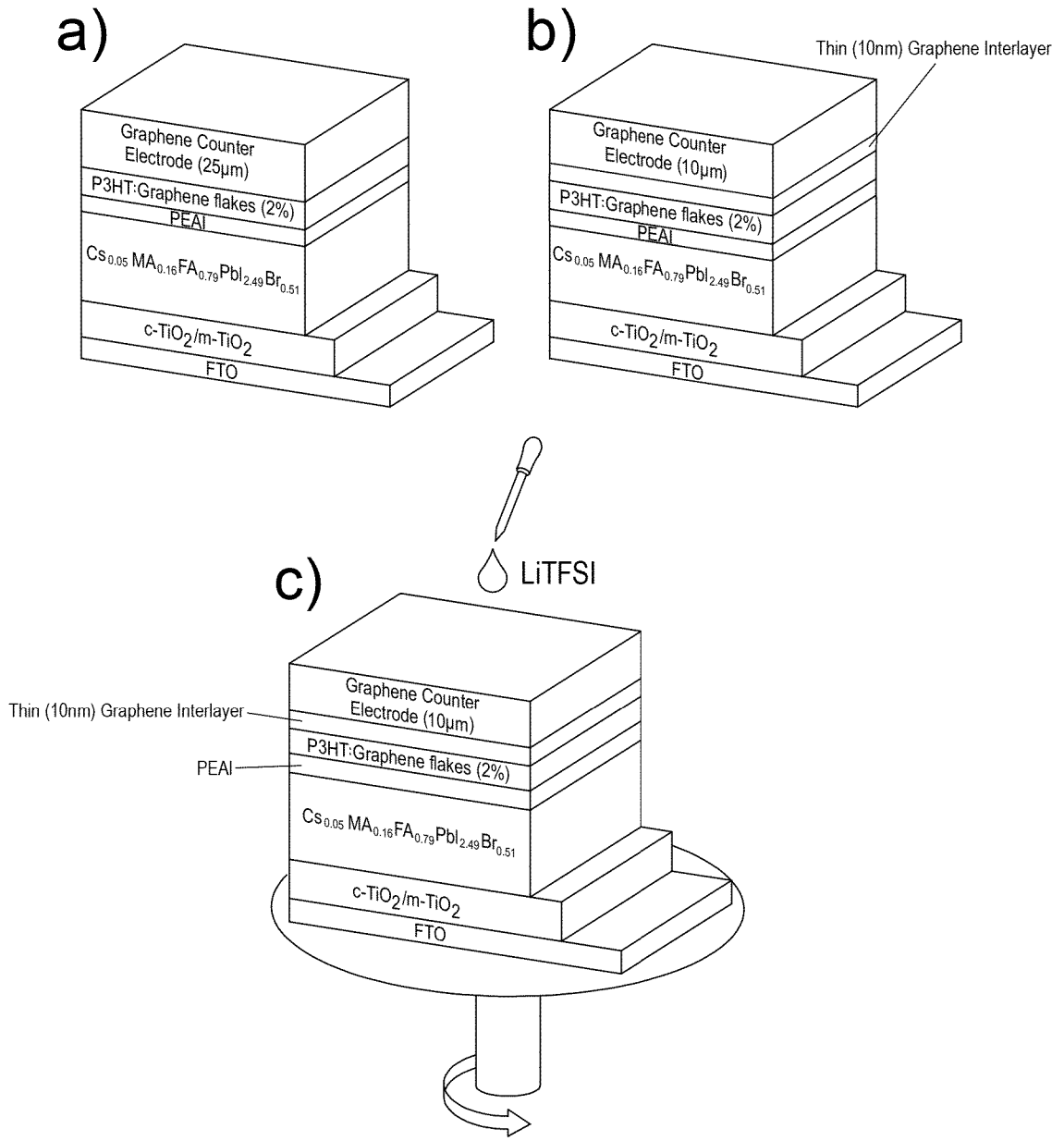

a)
Graphene Counter Electrode (25µm)
P3HT:Graphene flakes (2%)
PEAI
$Cs_{0.05}MA_{0.16}FA_{0.79}PbI_{2.49}Br_{0.51}$
$c\text{-}TiO_2/m\text{-}TiO_2$
FTO
b)
Thin (10nm) Graphene Interlayer
Graphene Counter Electrode (10µm)
P3HT:Graphene flakes (2%)
PEAI
$Cs_{0.05}MA_{0.16}FA_{0.79}PbI_{2.49}Br_{0.51}$
$c\text{-}TiO_2/m\text{-}TiO_2$
FTO
c)
LiTFSI
Thin (10nm) Graphene Interlayer
PEAI
Graphene Counter Electrode (10µm)
P3HT:Graphene flakes (2%)
$Cs_{0.05}MA_{0.16}FA_{0.79}PbI_{2.49}Br_{0.51}$
$c\text{-}TiO_2/m\text{-}TiO_2$
FTO

Fig. 14

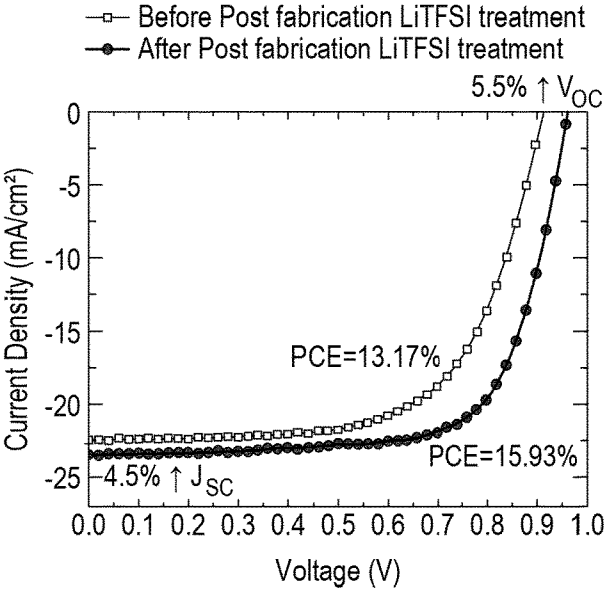

Before Post fabrication LiTFSI treatment
After Post fabrication LiTFSI treatment
5.5% ↑ V_{OC}
Current Density (mA/cm²)
PCE=13.17%
PCE=15.93%
-4.5% ↑ J_{SC}
Voltage (V)

Fig. 15

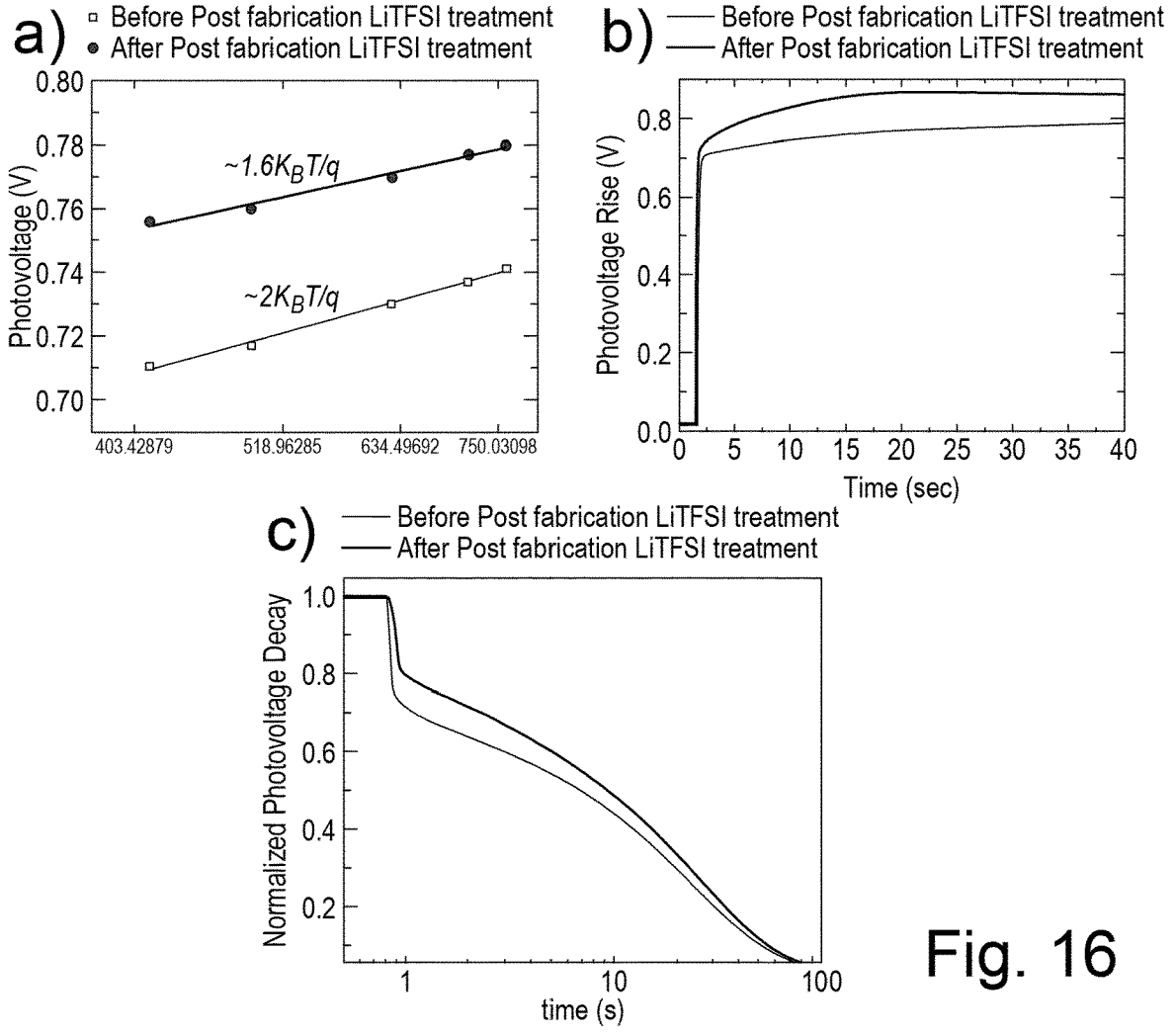

a)
Before Post fabrication LiTFSI treatment
After Post fabrication LiTFSI treatment
Photovoltage (V)
~1.6K_BT/q
~2K_BT/q
b)
Before Post fabrication LiTFSI treatment
After Post fabrication LiTFSI treatment
Photovoltage Rise (V)
Time (sec)
c)
Before Post fabrication LiTFSI treatment
After Post fabrication LiTFSI treatment
Normalized Photovoltage Decay
time (s)

Fig. 16

PEROVSKITE SEMICONDUCTOR DEVICES

[0001] The project leading to this application has received funding from the European Union's Horizon 2020 research and innovation programme under the Graphene Flagship grant agreement No 785219 and the Marie Sklodowska-Curie grant agreement No 747381.

FIELD OF THE INVENTION

[0002] The present invention relates to perovskite based semiconductor devices. The semiconductor devices include solar cells and light-emitting devices.

BACKGROUND TO THE INVENTION

[0003] Perovskite based semiconductor devices have been previously described, for example in WO2015166066, WO2016083783 and WO2017001542. There is significant interest in the use of metal halide perovskite devices due to their high efficiencies for low-cost.

[0004] For example, metal halide perovskite solar cells (PSCs) are considered the most promising photovoltaic (PV) technology for low cost power generation due to their high PV efficiency and solution processability. PSC potential is tremendous as halide perovskite semiconductors have complementary absorption spectra compared to silicon (Si), and thus tandem solar cells can be realized by stacking a PSC on top of the Si solar cell, significantly improving in this way the efficiency of the already established Si photovoltaics.

[0005] However, there are continuing challenges towards the commercialisation of PSCs, including the low operational stability that these devices present in ambient conditions, the use of expensive components including metallic electrodes (gold or silver) and hole transporting materials (spiro-MeOTAD and PTAA), and the need for high processing conditions including high temperature ultra-high vacuum deposition equipment. These complexities combine to increase the manufacturing cost and complexity and decreases the scalability of device fabrication.

[0006] Thus, there remains a need for new perovskite based semiconductor devices to overcome or mitigate some or all of the issues identified above.

SUMMARY OF THE INVENTION

[0007] The applicant has found that using particular electrodes together with doped injection layer(s) and a perovskite active layer according to the present invention provides semiconductor devices with enhanced properties.

[0008] According to an aspect of the present invention there is provided a semiconductor device comprising:

[0009] a first electrode comprising conductive material, wherein the conductive material is deposited by ink deposition (for example, layered material inks such as graphene and/or graphite), or wherein the conductive material comprises CVD grown graphene or carbon nanotubes;

[0010] a first charge transportation layer, wherein the first charge transportation layer is doped with the conductive material of the first electrode;

[0011] an optional insulation layer;

[0012] a perovskite active layer;

[0013] a second charge transportation layer;

[0014] and a second electrode.

[0015] The devices according to the present invention have improved performance over existing devices. Improved performance may be increased efficiency (for example Power Conversion Efficiency or PCE). Improved performance may be increased device stability. Manufacturing devices according to the present invention can reduce production cost thereby leading to overall improvements in device cost effectiveness.

[0016] A further advantage of providing the conductive material in both the first electrode and as a dopant in the first charge transportation layer is to enhance the low initial conductivity of the first charge transportation layer (which may be a hole transporting injection layer) and to form a better network for hole extraction from the perovskite active layer.

[0017] By avoiding the need for a standard metal electrode yet maintaining sufficient performance levels can improve device scalability and can significantly increase speed of production, for example, by avoiding the need for thermal evaporation process that is required for the metal-based electrodes. By utilising the present invention, for example, printable electrodes can be made with commercially attractive efficiencies and cost.

[0018] In a further aspect, there is provided a method of making a semiconductor device comprising applying the first electrode to the device via ink deposition, wherein the ink comprises conducive material dispersed in a solvent, wherein the solvent is selected to be compatible with the perovskite layer, wherein the solvent is selected from IPA, ethanol and ethyl acetate.

[0019] Optionally, the first electrode may be a nanoplate electrode which is a printed nanoplate electrode, wherein the nanoplates may comprise microfluidized graphite or graphene. Advantageously, this allows for a low cost and fully-printable method of fabricated a PSC.

[0020] By utilising a conductive material dispersed in a solvent (e.g. an ink) to form the first electrode improves device scalability and can significantly increase speed of production, for example, by avoiding the need for thermal evaporation process that is required for the metal-based electrodes. By utilising the present invention, devices based on printable electrodes can be made with commercially attractive efficiencies and cost. The use of specific solvents in the present invention protects the other layers in the device.

[0021] In a further aspect there is provided a method of producing a semiconductor device comprising a first electrode, the method comprising doping the charge transportation layer adjacent to the first electrode with conductive material of the first electrode. For example, using a graphene/graphite electrode and doping the adjacent charge transportation layer with graphene/graphite.

[0022] Such an approach, improves the efficiency of the device, for example the power conversion efficiency (PCE).

[0023] In a further aspect of the present invention, there is provided a semiconductor device comprising: a first electrode; a first charge transportation layer, wherein the first charge transportation layer is doped with conductive material of the first electrode; an insulation layer; and a perovskite active layer. It has been found that this combination has particularly advantageous properties, both in terms of efficiency and stability.

[0024] In a further aspect of the present invention, there is provided a semiconducting device comprising a charge

injection layer doped with material used to form the adjacent electrode. Such an approach improves performance of the device.

[0025] In a further aspect there is provided a solar cell comprising a semiconductor device according to the present invention.

[0026] In a further aspect there is provided an LED comprising a semiconductor device according to the present invention.

BRIEF DESCRIPTION OF THE FIGURES

[0027] FIG. **1** shows an exemplary device according to the present invention.

[0028] FIG. **2** shows a further exemplary device according to the present invention.

[0029] FIG. **3** shows viscosity as a function of shear rate for an ink made according to the present invention.

[0030] FIG. **4** shows the stability of nanoplate electrode inks over several months.

[0031] FIG. **5** shows images of fresh ink vs ink which has been stored at room temperature for several months.

[0032] FIG. **6** shows a schematic diagram showing charge transportation layer doping.

[0033] FIG. **7** shows (a) the halide perovskite film on glass, (b) the as blade coated graphene ink on top of the perovskite layer, (c) the perovskite/graphene heterostructure after the curing of the ink in room temperature and (d) the thickness of the as printed and cured microfluidized graphene film.

[0034] FIG. **8** shows an I-V curve for a device made according to the present invention.

[0035] FIG. **9** shows stability tests of PSCs made according to the present invention vs a device with an Au back electrode (exposing the devices without encapsulation in harsh conditions, at 60° C./60% relative humidity).

[0036] FIG. **10** shows an I-V curve for a device made according to the present invention in comparison with a device which has a gold back electrode but is otherwise identical.

[0037] FIG. **11** shows a stability test of a PSC according to the present invention exposing the device in ambient conditions without encapsulation.

[0038] FIG. **12** shows as-prepared graphene interlayer ink with a nanoplates concentration of 1 mg/ml in IPA.

[0039] FIG. **13** shows (a) the front side, (b) the back side and (c) a schematic of the front side of a PSC fabricated with a graphene counter electrode according to the present invention.

[0040] FIG. **14** shows (a) an exemplary device according to the present invention with a 25 μm thick graphene counter electrode, (b) an exemplary device according to the present invention with a graphene interlayer and a 10 μm thick graphene counter electrode and (c) an exemplary device according to the present invention undergoing a post device fabrication treatment with LiTFSI/ACN solution.

[0041] FIG. **15** shows I-V curves of devices fabricated according to the present invention before and after post-fabrication LiTFSI treatment.

[0042] FIG. **16** shows (a) photovoltage vs light Intensity, (b) photovoltage rise and (c) normalized photovoltage decay of devices fabricated according to the present invention before and after post-fabrication LiTFSI treatment.

DETAILED DESCRIPTION

[0043] The following embodiments apply to all aspects of the present invention. The present invention provides a semiconductor device comprising: a semiconductor device comprising: a first electrode comprising conductive material, wherein the conductive material is deposited by ink deposition (for example, layered material inks such as graphene and/or graphite), or wherein the conductive material comprises CVD grown graphene or carbon nanotubes; a first charge transportation layer, wherein the first charge transportation layer is doped with the conductive material of the first electrode; an optional insulation layer; a perovskite active layer; a second charge transportation layer; and a second electrode.

[0044] The term "semiconductor device" may be a solar cell. The semiconducting device may be a light emitting device. The semiconductor device may be a transistor, photodetector, or laser.

[0045] In a yet further embodiment, there is provided a solar cell incorporating a semiconductor device as described herein. In a yet further embodiment, there is provided a light emitting device incorporating a semiconductor device as described herein.

[0046] The "first electrode" according to the present invention is deposited by ink deposition or comprises CVD grown nanomaterials. Suitable electrodes are deposited by printable conductive inks. Such inks may be perovskite compatible inks, including low temperature processing and solvent compatible.

[0047] Suitable conductive materials for use in a printable conductive ink include layered material inks. Suitable layered material inks include graphene, graphite and MXenes. Layered materials may be nanoplates, including graphite/graphene nanoplates. The first electrode may be a first nanoplate electrode.

[0048] Suitable conductive materials for use in a printable conductive ink also include carbon inks (such as carbon black, carbon/graphite, graphite and carbon nanotubes inks).

[0049] Suitable conductive materials for use in a printable conductive ink also include metal inks, for example nanowire inks, including silver and copper inks, for example silver and copper nanowire inks.

[0050] Once deposited, the first electrode will comprise the conductive material, for example graphene, graphite, carbon nanotubes, silver or copper nanowires and the like.

[0051] In an alternative embodiment, the first electrode is not deposited by ink deposition but instead comprises chemical vapour deposition (CVD) grown nanomaterials including graphene or carbon nanotubes.

[0052] The first electrode therefore comprises a number of materials, mainly nanomaterials, which have been deposited by CVD but more preferably via ink deposition. Once deposited, the layer forms a suitable electrode.

[0053] In a preferred embodiment, the first electrode is a first nanoplate electrode. In a further embodiment, the first electrode is a layered material electrode. In a yet further embodiment, the first electrode is a graphene/graphite nanoplate electrode.

[0054] The "first nanoplate electrode" comprises a layered material, including graphite/graphene nanoplates. Generally, individual nanoplates will be understood to comprise a plurality of stacked layers, forming plates, i.e. a structure whose width is greater than its thickness. This may also be

referred to as the aspect ratio. A graphite nanoplate may also be defined as 'single/few layer graphene'.

[0055] For the avoidance of doubt, the term first nanoplate electrode means an electrode comprising nanoplates. The electrode itself is not nanoscaled but comprises nanoscale material.

[0056] Further generally, a nanoplate generally relates to a high aspect ratio structure, i.e. having a length to thickness ratio of greater than around 5. A thickness of an individual nanoplate may be less than around 100 nm and greater than around 500 nm. When formed as an electrode, the nanoplates may form or resemble a nematic structure, i.e. relating to a state in which the nanoplates may generally, or locally, be oriented in parallel but not arranged in well-defined planes (such as layers in bulk graphite).

[0057] Graphite nanoplates, which when in a bulk material, or during fabrication, may be referred to as microfluidized graphite, comprise a plurality of layers of stacked graphene. Preferably, this may correspond to a thickness of around 10 nm or less, or around 20 individual stacked graphene layers or less. Most preferably, the layers are pristine graphite and the nanoplates are graphite nanoplates.

[0058] Nevertheless, it will be understood that graphene nanoplates may comprise many more, or fewer layers of stacked graphene. Advantageously, graphite/graphene nanoplates with a very small thickness (e.g. single/few layers graphene, less than 10 layers thick), to achieve useful concentrations of only single/few layers graphene are achievable using high pressures (>30 kpsi) during an exfoliation step comprised in the fabrication of the microfluidized graphite.

[0059] US 2018/0312404 (the contents of which are hereby incorporated by reference) discloses methods to produce dispersions of layered materials via high shear microfluidic processing. Such layered materials are suitable for use in the present invention.

[0060] In a preferred embodiment, the first nanoplate electrode is produced from a conductive ink comprising graphite/graphene nanoplates. Said conductive ink comprises nanoplates dispersed in a suitable carrier liquid.

[0061] The nanoplate electrode may be printed from a precursor substance, which may be a dispersion comprising concentrations of graphene nanoplates of around 5 g/L or more in a suitable solution. This forms a viscous paste which allows subsequent printing by e.g. screen and flexo printing, spray coating, doctor blade method, and the like. Advantageously, the high viscosity provided by the high concentration prevents flocculation (i.e. unfavourable clumping) in the nanoplates. More preferably, the layered material (e.g. graphite nanoplates) is present in the precursor dispersion at a concentration of around at least 10 g/L.

[0062] Preferably, conductive inks by processing graphite with a microfluidizer resulting to graphite/graphene nanoplates.

[0063] The present invention allows the production of stable nanoplates from a layered material by microfluidization, without the need for stabilizing agents. This allows the production of pure dispersions of high conductivity (sheet resistance below 5 Ohm per square for ~20 pm films) in case of graphite/graphene nanoplates.

[0064] Purity and lack of additives allows the application of these dispersions at room temperature or low temperature processing without the need of high temperature processing as annealing for endowing high conductivity, which enables their use on devices where further materials or elements don't withstand elevated processing temperatures, as the case of halide perovskite absorbers and organic hole transporting materials.

[0065] Dispersions can have concentrations of 5 g/L or more, forming preferably viscous pastes that can be applied by screen and flexo printing, spray coating and doctor blade method.

[0066] In a preferred embodiment, the nanoplates are dispersed in a solvent which is compatible with other layers in the device, such as the charge transport layer(s) or active perovskite layer. The solvent may be selected so that the material used for the charge transport layer is insoluble. The solvent may be selected to be compatible with the perovskite layer. The solvent may be selected to be compatible with the microfluidizer equipment. A suitable solvent is IPA. Further suitable solvents include ethanol and ethyl acetate.

[0067] Accordingly, in an aspect of the present invention there is provided a method of manufacturing a semiconductor device having a nanoplate electrode wherein the nanoplate electrode is applied via a conductive ink and the conductive ink uses a perovskite compatible and/or charge transport layer compatible solvent, for example IPA, ethanol and ethyl acetate, most preferably IPA.

[0068] For example, the direct microfluidization of graphite in IPA allows the production of stable graphite/graphene nanoplates ink without the need of stabilizing agents (which is beneficial for the low temperature processing needed).

[0069] As a further example, P3HT solubility in IPA is <0.1 mg/mg so the injection layer protects all the other layer underneath.

[0070] The "first charge transportation layer" may be formed of a semiconducting material. In a further embodiment, the first charge transportation layer may be formed of an organic semiconducting material.

[0071] The first charge transportation layers may be a hole transporting organic or inorganic semiconducting material. The material may be selected from the group consisting of PEDOT:PSS, PANI (polyaniline), polypyrrole, optionally substituted, doped poly(ethylene dioxythiophene) (PEDOT).

[0072] Organic hole transport materials include Poly(triaryl amines) e.g. PTAA (poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine]); benzodithiophene (BDT) based polymer; polymer,poly(p-phenylene) PPP; lead phthalocyanine (PbPc); poly(9,9-dioctylfluorene-co-N-(4-(3-methylpropy-Wdiphenylamine) (TFB); polythiophene (PT); poly(4,4'-bis (N-carbazolyl)-1,1'-biphenyl) (PPN).

[0073] Inorganic hole transport materials include nickel oxide (NiO); copper thiocyanate (CuSCN); copper iodide (CuI); $CuInS_2$ (quantum dots); ternary oxide: $Li_{0.05}Mg_{0.15}Ni_{0.8}O$.

[0074] The first charge transportation layer may be small organic molecule HTMs, including spiro OMeTAD; FDT (triazatruxene and others based on the dithiophene core); and PCP-TPA, a triphenyl amine based compound.

[0075] The first charge transportation layer may be a hole transporting organic semiconducting material selected from the group consisting of polyfluorenes (preferably F8, TFB, PFB or F8-TFB) or Spiro-OMeTAD or polycarbazole (preferably poly(9-vinylcarbazole)) or 4,4'-Bis(N-carbazolyl)-1,1'-biphenyl, or poly(3-hexylthiophene-2,5-diyl) (P3HT).

[0076] In a preferred embodiment, the first charge transportation layer is poly(3-hexylthiophene-2,5-diyl) (P3HT).

In a preferred embodiment, the first charge transportation layer is Poly[2,2""-bis[[(2-butyloctyl)oxy]carbonyl][2,2':5',2":5",2'"-quaterthiophene]-5,5'"-diyl] (PDCBT). In a preferred embodiment, the first charge transportation layer is poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA). In a preferred embodiment, the first charge transportation layer is copper thiocyanate (CuSCN). In a preferred embodiment, the first charge transportation layer is Diketopyrrolopyrrole (pDPP5T-2).

[0077] More preferably, the first charge transportation layer is P3HT, PDCBT, or CuSCN.

[0078] In a most preferred embodiment, the first charge transportation layer is P3HT. In a most preferred embodiment, the first charge transportation layer is PDCBT. In a most preferred embodiment, the first charge transportation layer is CuSCN.

[0079] In a preferred embodiment the first charge transportation layer is a doped charge injection layer. In a preferred embodiment, the charge transportation layer is doped with the first electrode material. For example, a device using a graphene/graphite layered material in the first electrode may have a charge injection layer doped with the same layered material.

[0080] In greater detail, in a further preferred embodiment, the first charge transportation layer may be a hole injection layer (or more generally a hole transporting material), which is disposed adjacent to the first electrode. The first electrode may comprise graphene/graphite nanoplates and the first charge transportation layer is doped with graphene/graphite nanoplates. Advantageously, the effect of doping the hole injection/transportation layer with graphene is to provide a non-hygroscopic dopant whilst simultaneously achieving a high conductivity.

[0081] As mentioned, conventional PSC devices are known to use Li-salts dopants in the hole transportation layers, which are detrimental to solar cell long-term stability, and relatively expensive. Using graphene/graphite nanoplatelets and the like may obviate the need for such Li-salts in hole transportation layers.

[0082] Further advantageously, the graphene/graphite nanoplatelets (or microfluidized graphite) or other conductive materials may be printed to form the electrode, which allows for a fully-printable PSC device.

[0083] In a preferred embodiment, charge transportation layer is doped with 0.5 to 3%, 0.5 to 2.5%, 1 to 3%, 1 to 2%, 0.5, 1, 1.5, 2, 2.5 or 3%.

[0084] In a preferred embodiment, the charge transportation layer is doped with the same material as the first electrode. However, in other embodiments, a different but suitable charge carrying doping material may also be used. In a preferable example, the first charge transportation layer (which may be a hole transporting layer) is doped with a small amount (around 2%) of low concentration (e.g. around 2 mg/ml) microfluidized graphite ink, where the first electrode also comprises a much higher concentration (up to 100% concentration) of the same microfluidized graphite (i.e. graphene nanoplates.)

[0085] As such, according to the present invention, there is provided a semiconducting device comprising a charge injection layer doped with the electrode material. In a preferred embodiment, the electrode material is graphene/graphite. In a further preferred embodiment, the charge injection layer is a hole injection layer. In a further preferred embodiment, the hole injection layer is P3HT. In a yet further embodiment, the charge injection layer is doped with 0.5 to 3%, 0.5 to 2.5%, 1 to 3%, 1 to 2%, 0.5, 1, 1.5, 2, 2.5 or 3%. In a preferred embodiment, the active layer is a perovskite. In a further preferred embodiment, there is an insulating layer between the active layer and the doped charge injection layer.

[0086] The "insulation layer" may be formed of an insulating polymer and is selected from the group consisting of poly(ethyleneimine) (PEI), polyethylenimine-ethoxylated (PEIE), polystyrene (PS), poly(methylmethacrylate) (PMMA) and organic halide salts, for example phenethylammonium iodide (PEAI), Guanidinium iodide (GuI) Guanidinium bromide (GuBr), n-Butylamonium iodide (BAI), n-Butylammonium bromide (n-BABr) and ethylenediammonium diiodide ($EDAI_2$). In a preferred embodiment, the insulation layer is an organic halide salt. In a further preferred embodiment, the insulation layer is phenethylammonium iodide (PEAI).

[0087] The insulating layer(s) may be deposited by any suitable means including atomic layer deposition, ALD, spin coating or thermal evaporation etc.

[0088] In an embodiment, a thin layer of <30 nm of a material selected molybdenum trioxide and tungsten trioxide is deposited between the electrode and the perovskite layer, between a charge transportation layer and electrode, between the electrode and a charge transportation layer, between the perovskite layer and a charge transportation layer or between the perovskite layer and an electrode.

[0089] The "perovskite active layer" may comprise a halide perovskite. The halide perovskite may be an organic metal halide perovskite or an inorganic metal halide perovskite or a hybrid organic-inorganic metal halide perovskite material. The invention is not particularly limited in the choice of perovskite active layer provided it has the desired properties. As such, in embodiments of the invention any suitable perovskite layer may be used. The perovskite may be a 3D perovskite. The perovskite may have lower dimensionality. The perovskite may be a 2D perovskite. The perovskite may be a 1D perovskite. The perovskite may be a quasi-2D perovskite (that is a 2D/3D perovskite).

[0090] In embodiments, the perovskite may be an organic metal halide perovskite, and may have an AMX_3 structure, where A is a monovalent organic cation or a monovalent metal cation, M is a divalent cation and X is a halide anion.

[0091] In an embodiment, A may be a monovalent organic cation or a monovalent metal cation.

[0092] A may be dual cationic with an $A_{1-i}B_i$ structure, wherein: A and B are each a monovalent organic cation or monovalent metal cation, where A and B are different; and i is between 0 and 1.

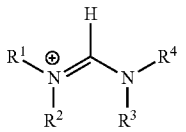
[0093] A may be triple cationic with an $A_\alpha B_\beta C_\gamma$ structure, wherein: A, B and C are each a monovalent organic cation or monovalent metal cation, where A, B and C are different; and α, β and γ combined equal 1.

[0094] A may be quadruple cationic with an $A_\alpha B_\beta C_\gamma D_\delta$ structure, wherein: A, B, C and D are each a monovalent organic cation or monovalent metal cation, where A, B, C and D are different; and α, β, γ and δ combined equal 1.

[0095] The monovalent organic cation may be a primary, secondary or tertiary ammonium cation $[HNR^1R^2R^3]^+$, wherein each of R^1, R^2 and R^3 may be the same or different and is selected from hydrogen, an unsubstituted or substituted C_1-C_{20} alkyl group and an unsubstituted or substituted C_5-C_{18} aryl group. Examples of suitable substituents for the

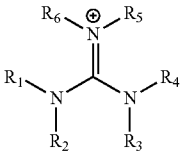
alkyl groups are alkoxy groups having from 1 to 20 carbons atoms, hydroxyl groups, mono and dialkylamino groups wherein each alkyl group may be the same or different and has from 1 to 20 carbon atoms, cyano groups, nitro groups, thiol groups, sulphinyl groups, sulphonyl groups and aryl groups having from 5 to 18 carbon atoms. Examples of suitable substituents for the alkyl groups are alkyl groups having from 1 to 20 carbon atoms, alkenyl and alkynyl groups each having from 2 to 20 carbon atoms, alkoxy groups having from 1 to 20 carbons atoms, haloalkyl groups having from 1 to 20 carbon atoms, hydroxyl groups, mono and dialkylamino groups wherein each alkyl group may be the same or different and has from 1 to 20 carbon atoms, cyano groups, nitro groups, thiol groups, sulphinyl groups and sulphonyl groups.

[0096] In embodiments, the monovalent organic cation may be of the form $[R^1R^2N—CH═NR^3R^4]^+$:



[0097] wherein each of R^1, R^2, R^3 and R^4 may be the same or different and is selected from hydrogen, an unsubstituted or substituted C_1-C_{20} alkyl group and an unsubstituted or substituted C_5-C_{18} aryl group.

[0098] In embodiments, the monovalent organic cation may be of the form $(R^1R^2{}_N)(R^3R^4N)C═N^+R^5R^6$:



[0099] wherein each of R^1 R^2, R^3, R^4, R^5 and R^6 may be the same or different and is selected from hydrogen, an unsubstituted or substituted C_1-C_{20} alkyl group and an unsubstituted or substituted C_5-C_{18} aryl group.

[0100] In embodiments, the monovalent metal cation may be an alkali metal cation.

[0101] In embodiments, the monovalent metal cation is caesium (Cs^+), rubidium (Rb^+) and/or potassium (K^+).

[0102] In an embodiment, M is a divalent cation.

[0103] In a further embodiment, M has the structure $M_{1-j}N_j$ wherein M and N are each a divalent metal cation; and j is between 0 and 1.

[0104] In a further embodiment, M has the structure $M_\epsilon N_\zeta O_\eta$ structure, wherein: M, N and O are each a divalent metal cation, where M, N and O are different; and ϵ, ζ and η combined equal 1.

[0105] The divalent cation M may be a divalent metal cation, such as, but not limited to, tin (Sn^{2+}), lead (Pb^{2+}), cobolt (Co^{2+}) and/or zinc (Zn^{2+}).

[0106] In an embodiment, X is a halide anion.

[0107] In a further embodiment, X has the structure $X_{3-k}Y_k$, wherein X and Y are each a halide anion, where X and Y are different; and k is between 0 and 3.

[0108] In a yet further embodiment, X has the structure $X_\alpha Y_\beta Z_\gamma$ structure, wherein: X, Y and Z are each a halide anion, where A, B and C are different; and α, β and γ combined equal 1.

[0109] Halide anions may be chosen from chloride, bromide, iodide, and fluoride, and a chalcogenide anion may be chosen from sulphide, selenide, arsenide and telluride.

[0110] Preferably, the halide anions may be selected from chloride, bromide, iodide, and fluoride. Preferably at least one of X, Y or Z includes bromide.

[0111] All combinations of the above described perovskites are encompassed by the present invention as described above. For example, the perovskite may take the form:

	A	M	X_3
1	A	M	X_3
2	$A_{1-i}B_i$	M	X_3
3	$A_\alpha B_\beta C_\gamma$	M	X_3
4	A	$M_{1-j}N_j$	X_3
5	$A_{1-i}B_i$	$M_{1-j}N_j$	X_3
6	$A_\alpha B_\beta C_\gamma$	$M_{1-j}N_j$	X_3
7	A	M	$X_{3-k}Y_k$
8	$A_{1-i}B_i$	M	$X_{3-k}Y_k$
9	$A_\alpha B_\beta C_\gamma$	M	$X_{3-k}Y_k$
10	A	$M_{1-j}N_j$	$X_{3-k}Y_k$
11	$A_{1-i}B_i$	$M_{1-j}N_j$	$X_{3-k}Y_k$
12	$A_\alpha B_\beta C_\gamma$	$M_{1-j}N_j$	$X_{3-k}Y_k$
13	A	M	$X_\alpha Y_\beta Z_\gamma$
14	$A_{1-i}B_i$	M	$X_\alpha Y_\beta Z_\gamma$
15	$A_\alpha B_\beta C_\gamma$	M	$X_\alpha Y_\beta Z_\gamma$
16	A	$M_{1-j}N_j$	$X_\alpha Y_\beta Z_\gamma$
17	$A_{1-i}B_i$	$M_{1-j}N_j$	$X_\alpha Y_\beta Z_\gamma$
18	$A_\alpha B_\beta C_\gamma$	$M_{1-j}N_j$	$X_\alpha Y_\beta Z_\gamma$

[0112] The perovskites may equally be quadruple cationic and/or ternary metals and the resultant permutations available thereof.

[0113] Particularly preferred are triple cationic perovskites. Also preferred are mixed halide perovskites.

[0114] The "second charge transportation layer" may be formed of a semiconducting material.

[0115] In a further embodiment, the second charge transportation layers may be formed of an organic semiconducting material.

[0116] The second charge transportation layers may be an electron transporting organic semiconducting material. The material may be selected from the group consisting of poly(fluorene)s, preferably F8, TFB, F8BT or F8-TFB AB copolymer (95:5 F8:TFB).

[0117] The electron transporting semiconducting material may be selected from Electron Transport Materials (ETLs) including inorganic ETLs like TiO_2; ZnO; SnO_2; ZrO_2; $SrTiO_3$; $ZnSnO_4$; or WO_3 or organic ETLs like PCBM: polystyrene; C60; PEHT; or polyethyleneimine (PEI) or poly(ethylenimine) ethoxylated (PEIE) or 2-Methoxyethanol; PCBM or PCBM:PMMA. The materials may be mesoporous films. Alternatively, the materials may be bulk/compact thin films.

[0118] The second charge transportation layers may be an electron transporting inorganic semiconducting material selected from the group consisting of titanium dioxide (TiO_2), zinc oxide (ZnO), magnesium zinc oxide (MgZnO) and aluminium-doped ZnO (AZO).

[0119] In a preferred embodiment, the second charge transportation layer is a TiO_2. In a preferred embodiment, the second charge transportation layer is a ZnO. In a

preferred embodiment, the second charge transportation layer is a SnO_2. In a preferred embodiment, the second charge transportation layer is a C60. In a preferred embodiment, the second charge transportation layer is a PCBM. In a preferred embodiment, the second charge transportation layer is a $ZnSnO_4$.

[0120] In a most preferred embodiment, the second charge transportation layer is a TiO_2. In a most preferred embodiment, the second charge transportation layer is a SnO_2. In a most preferred embodiment, the second charge transportation layer is a PCBM or PCBM:PMMA.

[0121] For the avoidance of doubt, the charge transportation layer(s) described herein (the first and or/second charge transportation layer) may include combinations of the materials outlined above. As an example, an electron transporting layer may comprise ZnO coated with PEIE. Further combinations include compact and/or mesoporous-TiO_2 coated with LiTFSI or C60, PCBM, PCBM:PMMA, PCBA, Benzoic acid.

[0122] In an embodiment, the device may include a TiO_2 electron transporting layer and a spiro MeOTAD hole transporting layer. The device may be a solar cell. In an alternative embodiment, the device may include a ZnO-PEIE electron transporting layer and a TFB hole transporting layer. The device may be a LED.

[0123] The "second electrode" may preferably be formed of a transparent, conductive material.

[0124] The second electrode may be formed of indium tin oxide (ITO), fluorine doped tin oxide (FTO), indium zinc oxide, graphene, carbon nanotubes and silver nanowires. The electrode may be formed from a metal. A metal could be up to 100-150 nm thick.

[0125] An example device according to the present invention is shown in FIG. **1**, which shows first electrode (**102**), first charge injection layer (**104**), insulation layer (**106**), perovskite active layer (**108**), second charge injection layer (**110**), second electrode layer (**112**). The first charge injection layer (**104**) may be a doped charge injection layer. The layer may be doped with the same material as the first electrode, for example, graphene.

[0126] Additional layers or regions may be present between each of these regions. For example, an insulation layer may be present between the perovskite active layer and second charge injection layer. However, typically, each region described is in contact with both the preceding and the succeeding region as disclosed herein. The present invention does not exclude the presence of additional layers. Indeed, an advantage of the present invention is that it can be incorporated into, for example, tandem solar cells. For the avoidance of doubt, the present invention describes a number of layers which have been identified as leading to advantageous properties. The invention does not preclude further layers to be present in the device. These further layers may be on either side of the layers described herein. These further layers may equally be between the layers described in the present invention. In this latter embodiment however, the further layers would not negate the technical effect seen with the current layer orientation as described in the present invention.

[0127] In an embodiment according to the present invention, the first electrode may have a layer thickness of >1 μm. In an embodiment, the first charge injection layer has a layer thickness of >10 nm. In an embodiment, the insulation layer has a layer thickness of <30 nm. In an embodiment, the active perovskite layer has a layer thickness of >100 nm. In an embodiment, the electron injecting layer has a layer thickness of >100 nm, for example compact (c-)TiO_2>10 nm; mesoporous (m-)TiO_2>100 nm. In an embodiment, the second electrode may have a layer thickness of >250 nm.

[0128] A further example device is shown in FIG. **2**. While the graphene is shown in the figure as being doped at 2%, this can be varied as described herein.

[0129] In embodiments of the present invention, an interlayer may be present between the first electrode and the first charge transportation layer. The "interlayer" according to the present invention may comprise a conductive material. Alternatively, the "interlayer" according to the present invention may comprise an ultrathin (below 5 nm) insulating film. The interlayer may be deposited by ink deposition or comprises CVD grown nanomaterials. A conductive interlayer may comprise any of the materials that have been described as suitable for forming the first electrode. An ultrathin insulating interlayer may comprise any of the insulating materials defined herein.

[0130] In an embodiment, the interlayer may comprise the same material as the first electrode. The interlayer material may be produced from a conductive ink comprising graphite/graphene nanoplates. Said conductive ink comprises nanoplates dispersed in a suitable carrier liquid. The interlayer may be printed from a precursor substance, which may be a dispersion comprising concentrations of graphene nanoplates in a suitable solution. Where the interlayer and the first electrode are both printed from a precursor substance, the concentration of graphene nanoplatelets of the precursor substance from which the interlayer is printed may be lower than the concentration of graphene nanoplatelets from which the first electrode is printed.

[0131] The concentration of graphene nanoplatelets of a precursor substance from which the interlayer is printed may be around 0.1 g/L to 5 g/L. Other ranges include 0.2 g/L to 4 g/L, 0.5 g/L to 3 g/L, 0.5 g/L to 2 g/L, 1 g/L to 5 g/L, around 1 g/L, 1 g/L or more.

[0132] An interlayer according to the present invention may be deposited by spin-coating.

[0133] In an embodiment, the interlayer may have a thickness of between around 2 to 50 nm. In a preferred embodiment, the interlayer may have a thickness of between around 2 to 40 nm, 2 to 30 nm, 5 to 20 nm, 5 to 15 nm or around 10 nm.

[0134] An interlayer as described herein may function as a conductive bridge between the first electrode and the first charge transportation layer. Without wishing to be bound by theory, an interlayer as described herein may also act as a scaffold during formation of the first electrode, which may lead to improved uniformity of the first electrode and improve device reproducibility. Inclusion of an interlayer as described herein may enable fabrication of a thinner first electrode in comparison with devices without interlayers without reducing the achievable PCE of the device. For example, it may be possible for the first electrode of a device with an interlayer to have a thickness of less than 5 μm with no loss of PCE compared with a device with a thicker first electrode and no interlayer. Preferably, the first electrode of a device with an interlayer has a thickness of around 10 μm.

[0135] In a preferred embodiment, the device may comprise an interlayer as defined herein between the first electrode and the first charge transportation layer, wherein the first electrode has a thickness of less than 25 μm, preferably

less than 20 μm, less than 15 μm, less than 12 μm, less than 10 μm, less than 8 μm, less 6 μm, around 1 to 25 μm, around 3 to 20 μm, around 5 to 15 μm, around 7 to 12 μm, around 5 μm, around 6 μm, around 7 μm, around 8 μm, around 9 μm, around 10 μm, around 11 μm, around 12 μm, around 13 μm, around 14 μm, around 15 μm; preferably around 10 μm. The interlayer may have a thickness of between around 2 to 40 nm, 2 to 30 nm, 5 to 20 nm, 5 to 15 nm or around 10 nm.

[0136] In embodiments of the present invention, a metal salt or salts with electron accepting (p-type doping) properties salt may be present at one or more interfaces between layers of the semiconductor device. Such devices may exhibit improved performance, including improved fill factors and/or improved PCEs, in comparison with devices without the presence of said metal salt at one or more interfaces between layers. Without wishing to be bound by theory, the improved performance may be due to an improved interfacial contact between layers of the semiconductor device, reduced trap-assisted recombination at the interface(s) and/or increased carrier lifetimes.

[0137] According to embodiments, metal salt may be present at an interface between the perovskite active layer and a layer of the semiconductor device adjacent the perovskite active layer, at an interface between the first charge transportation layer and a layer of the semiconductor device adjacent the first charge transportation layer and/or at an interface between the first electrode and a layer of the semiconductor device adjacent the first electrode. For example, the presence of metal salt at an interface may reduce the presence of gaps between layers of a device fabricated according to the present invention.

[0138] Metal salt may be introduced into a device fabricated according to the present invention following fabrication of the device. In an embodiment, metal salt may be introduced into the device by applying metal salt to the surface of the first electrode. In an embodiment, metal salt may be introduced into the device by depositing a solution comprising metal salt onto the first electrode. Said solution may comprise metal salt in acetonitrile (ACN). Said solution may be spin casted/infiltrated on top of the first electrode. Alternatively, the salt could be applied by solution processing or thermal evaporation.

[0139] Without wishing to be bound by theory, the solution may not penetrate the device further than an interface between the first electrode and the first interlayer or the first charge transportation layer.

[0140] It will be understood that depositing salt onto the completed device following device fabrication according to the present invention is not the same as applying salt to each layer of the device during the fabrication process. It will also be understood that a post-fabrication treatment with metal salt according to the present invention may lead to improvements in devices with or without an interlayer.

[0141] Any suitable metal salt with electron accepting (p-type doping) properties may be utilised in this embodiment of the invention.

[0142] The metal salt may be a lithium metal salt. An exemplary (but not limiting) lithium metal salt is bis(trifluoromethane)sulfonimide lithium (LiTFSI) salt.

[0143] The metal salt may be a cobalt metal salt. Exemplary (but not limiting) cobalt metal salts include tris(2-(1H-pyrazol-1-yl)pyridine)cobalt(III) (FK102), tris(2-(1H-pyrazol-1-yl)-4-tent-butylpyridine)cobalt(III) tri[hexafluorophosphate] (FK209) and bis(2,6-di(1H-pyrazol-1-yl)yridine)cobalt(III)tris(bis(trifluoromethylsulfonyl) imide) (FK269), tris[2-(1H-pyrazol-1yl)pyrimidine]cobalt (III) tri[bis(trifluoromethylsulfonyl)imide] (MY11), and bipyridine cobalt complexes.

[0144] The metal salt may be a copper metal salt. Exemplary (but not limiting) copper metal salts include CuI, CuSCN, copper(II)-pyridine complexes including bis[di(pyridin-2-yl)methane] copper(II) bis[bis(trifluoromethylsulfonyl) imide][$Cu(bpm)_2$] and bis[2,2'-(chloromethylene)-dipyridine] copper(II) bis[bis(trifluoromethylsulfonyl) imide][$Cu(bpcm)_2$], and $Cu(bpcm)_2$.

[0145] The metal salt may be a silver metal salt. Exemplary (but not limiting) silver metal salts include AgTFSI. The metal salt may be an iron metal salt. Exemplary (but not limiting) iron metal salts include $FeCl_3$.

[0146] Preferably, the metal salt is bis(trifluoromethane) sulfonimide lithium (LiTFSI) salt.

[0147] The invention will now be described with reference to the following non-limiting examples.

Materials and Fabrication Techniques

Materials

[0148] Unless otherwise stated, all other materials were purchased from Sigma-Aldrich.

[0149] FTO (TEC7), the precursor solutions for c-TiO2 (Acetyl Acetone and titanium diisopropoxide bis(acetylacetonate)), Li-TFSI powder, P3HT powder and all the solvents used (IPA, ethanol, DFM, DMSO, Chlorobenzene, Dichlorobenzene) were purchased from Sigma-Aldrich. 30 NR-D paste for m-TiO_2 layer, the organic salts for the perovskite solution preparation (methylammonium bromide and) formamidinium iodide and PEAI

[0150] powder were purchased from GreatCell Solar. All the other compounds for the perovskite solution preparation (PbI_2, $PbBr_2$ and CsI) were purchased from TCI. The Graphite powder was purchased from lmerys Graphite and Carbon.

Preparation of Nanoplate Electrode Ink

[0151] Suitable nanoplate electrode ink was made following the processes described in US 2018/0312404.

[0152] The high viscosity of the pastes prevents the flocculation of graphite/graphene nanoplates due to complex networking forming metastable colloidal suspensions. This can be seen from FIG. **3**, which shows the viscosity as a function of shear rate for an ink made according to the present invention.

[0153] Inks made according to the present invention are stable for several months exhibiting negligible degraded conductivity (sheet resistance slightly above 5 Ohm per square for ~20 μm films) compared to fresh dispersions. This can be seen from FIG. **4**. FIG. **4***a* shows a comparison of Sheet resistances for the fresh and old ink-based films. FIG. **4***b* shows the dependence of sheet resistance on the number of microfluidization cycles for fresh samples. Although slightly degraded over time, the sheet resistance of the aged ink-based film is still significantly lower compared to the commercial carbon ink after sintering at 400° C.

[0154] Preferably, dispersions according to the present invention are produced by 10 or more microfluidization

cycles, preferably 15 or more, 20 or more, 30 or more, 40 or more, 50 or more, 60 or more, or 70 or more microfluidization cycles.

[0155] Dispersions made according to the present invention can be stored at room temperature for several months. This can be seen from FIG. **5** which shows the long-term stability of graphite/graphene nanoplates inks made according to the present invention. Fresh ink is shown on the left image with old ink on the right.

Preparation of the Graphene Dispersion for Charge Transportation Layer Doping

[0156] A small amount (~1 ml) of the as microfluidized graphene ink was dried overnight at 80° C. to ensure the complete evaporation of the solvent (IPA). The as obtained graphene powder was dispersed in dichlorobenzene (DCB) with a concentration of ~2 mg/ml and ultrasonicated inside an ultrasonic bath for ~1 hour. As soon as a homogenous graphene dispersion was obtained, the graphene solution was mixed with Poly(3-hexylthiophene-2,5-diyl) (P3HT) powder at different wt % concentrations. Then Chlorobenzene (CB) was added to the P3HT:Graphene mixture to keep a constant ration between CB and DCB solvents. Finally, the P3HT:Graphene mixture in CB/DCB was ultrasonicated for ~30 minutes to ensure the proper mixing of the blend.

[0157] A schematic diagram showing charge transportation layer doping is shown in FIG. **6**.

[0158] In step b), preferably the amount of the ink that is dried should be at least 100 μl to ensure that there is sufficient quantity for the doping process of 1 ml of P3HT solution. The concentration of Graphene in DCB was varied: 0.1, 0.3, 0.5, 0.75, 1, 1.5, 2, and 5 mg/ml. Different Graphene/P3HT doping ratios were tested and also different DCB/CB ratios were tested (1, 2.5, 5, 7.5, 10, 15, 20 and 25%).The effect of different percentages of doping was investigated using a graphene electrode and a P3HT hole transportation layer doped with varying amounts of graphene. 0% doping resulted in a PV Power Conversion Efficiency (PCE) of 11.5%. Doping the charge transportation layer resulted in the following PCE values: 1% and 2% doping improved PCE to ~13% (2% doping was slightly better). 5% doping had PCE performance ~11.5%. 10% and 15% doping had PCE of ~5%.

[0159] In a preferred embodiment, the charge transportation layer is doped with between 0.1 to 5% of the nanoplate material (e.g graphene/graphite). Preferably, the charge transportation layer is doped with 0.5 to 3%, 0.5 to 2.5%, 1 to 3%, 1 to 2%, 0.5, 1, 1.5, 2, 2.5 or 3% of the nanoplate material.

Solar Cell Fabrication

[0160] The solar cells were fabricated on Fluorine doped Tin Oxide (FTO) glass substrates (Aldrich, 7 Ohm/sq) patterned by wet etching with zinc powder and concentrated hydrochloric acid. Afterwards, the patterned glass/FTO substrates were cleaned ultrasonically with detergent in DI water, acetone and isopropyl alcohol. The compact TiO_2 (c-TiO_2) layer was deposited on the preheated at 450° C. glass/FTO substrates by spray pyrolysis. The mesoporous TiO_2 (m-TiO_2) solution (30 NR-D in ethanol) was spin-coated on top of the c-TiO_2 film, followed by a sintering step at 450° C. for 30 minutes. The doping of m-TiO_2 was accomplished by spin-coating a 0.1M Li-TFSI solution in acetonitrile followed by an additional sintering step at 450° C. for 30 minutes. See: F. Giordano et al, Nat. Commun. 2016, 7, 10379. After cooling down to 150° C., the samples were transferred inside a nitrogen filled glove box and the triple-cation lead-based mixed halide precursor solution was spin-coated on top of the m-TiO_2 layer (using a double spinning program) followed by the anti-solvent quenching step with CB.

[0161] Immediately after, to convert the spin-coated precursor film to perovskite, the samples we placed on a hot plate at 100° C. for 60 minutes. See M. Saliba et al, Energy Environ. Sci. 2016, 9, 1989. After cooling the samples down to room temperature, a phenylethylammonium iodide solution was spin-coated on top of the perovskite film, as a thin passivation layer. Subsequently, a P3HT in CB/DCB solution (undoped or Graphene doped at different Wt % concentrations) was spin-coated on top of the PEAI passivated perovskite film. Finally, the devices were completed by doctor blade coating of the microfluidized graphite on top of the P3HT or P3HT:Gr layer. The thickness of the wet microfluidized graphite film was set to 1-1.5 mm, which after the drying process was converted to a ~20 μm thick film. The deposition of the paste was realized in inert atmosphere and immediately afterwards, the samples were annealed for approximately 30 minutes at 80° C. to achieve good interfacial contact between the graphene electrode and the P3HT or P3HT:Gr layer. The devices were left without encapsulation for the characterization tests in ambient conditions.

Characterization of the Devices

[0162] The devices were placed under a solar simulator with one-sun light intensity (100 mW/cm^2, calibrated using a Si reference cell) and the Current-Voltage Curves were measured using a source meter (Keithley, 2400). The stability tests were conducted in ambient conditions either at room temperature or at 60° C./60% relative humidity inside a Climatic Chamber (Weiss WKL).

Discussion

[0163] As it can be seen, the present invention utilises highly conductive (FIG. **4**) and stable (FIG. **5**) inks that can be cured at room temperature (or preferably low temperatures, i.e. 80° C.) and present significantly lower sheet resistance compared to other similar materials used in PV devices, for example porous carbon-black. In order to test its compatibility with PSC fabrication, ink printability was tested together with resultant halide perovskite stability. The resultant structure during various stages of manufacture are shown in FIG. **7**.

[0164] By applying (printing) this new ink formulation for the preparation of a microfluidized graphite layer (~20 μm thickness) on top of the perovskite layer, it is possible to avoid degradation of the perovskite layer. This is due to the fact that the ink is processed from a perovskite compatible solvent (isopropyl alcohol) when dried in nitrogen filled glove box and is room-temperature or low temperature (if required) curable.

[0165] A process allowing room-temperature curing avoids degradation of the perovskite active layer which is sensitive to high temperature degradation. The present invention therefore allows for low temperature preparation of semiconductor devices by utilising conductive inks based

on compatible solvents. For example, devices can be cured at temperatures below 100° C., preferably below 80° C.

[0166] Subsequently, PSCs with the typical mesoscopic architecture were prepared as described herein to produce a device with the following architecture: FTO/c-TiO_2/m-TiO_2/Perovskite/PEAI/P3HT:Gr/Gr-Electrode). Following the process described above, the microfluidized graphite ink was printed on the samples and then cured at 80° C. to complete the device fabrication. The as prepared PSC with the graphene-based back electrode was then exposed to a solar simulator and the characteristic I-V curves were obtained to calculate the devices photovoltaic performance. The results are shown in FIG. **8** and it can be seen that the device achieves a remarkable PCE of 13.23%.

[0167] The optimisation of semiconductor devices according to the present invention achieves, in a PSC, remarkably high PCEs and significantly higher than PCE of ~11.5% achieved in the prior art. This improvement in PCE is due to the use of the features of the present invention and represents around the highest ever reported for a fully printable PSC.

[0168] The present invention also leads to a significant reduction in cost due to the printable conditions available for manufacture. This allows for cost-effective scalable processes to manufacture devices according to the present invention. Considering, for example, PSCs, reducing the fabrication costs can ensure the devices become cost effective for energy generation.

[0169] As well as the advantageous performance and product costs, the devices according to the present invention were also tested to determine their durability. A device according to the present invention (having an FTO/c-TiO2/m-TiO2/Perovskite/PEAI/Spiro-Ometad/Au architecture) is tested against a device comprising a gold electrode and without the doping of hole transporting layer with graphene. These results are shown in FIG. **9**, which show stability tests of PSCs. A device according to the present invention comprising a 2% graphene doped P3HT hole injection layer and graphene back electrode made according to the present invention was tested against a similar device comprising a spiro OMeTAD (with Li-doping)/Au device. It can clearly be seen that the devices according to the present invention are significantly more stable compared to the devices with gold electrodes under a 60° C./60% relative humidity stress test. It can also be seen that the device according to the present invention even under these conditions is superior compared to the state-of-the-art standard PSCs (see for example, Domanski et al ACS Nano, 2016, 10, 6306-6314).

[0170] It is important to note that the devices according to the present invention were made without any encapsulation process to prevent oxygen/moisture diffusion within the device. Without wishing to be bound by theory, the thick graphene paste-based film may perform an encapsulation role.

[0171] In a further experiment, PCE was evaluated for a device according to the present invention (P3HT:Gr/Gr) against the identical device but using an Au back electrode (P3HT:Gr/Au). The results are shown in FIG. **10**. It can be seen that the devices with microfluidized graphite presented significantly higher photovoltaic efficiency compared to Au devices.

[0172] In a further experiment, stability of devices according to the present invention were further evaluated. FIG. **11** shows that devices according to the present invention do not degrade over more than 400 hours stability testing (D1 ISOS protocol, self-degradation). Indeed, their efficiency appears to increase.

[0173] In conclusion, the present invention has identified semiconductor devices with improved performance. Improved performance may be increased efficiency. Improved performance may be increased stability. The present invention has also identified semiconductor device manufacturing processes that reduce production cost.

[0174] The present invention avoids the need for traditionally deposited metal electrodes yet maintains sufficient performance levels. Utilising printable electrodes improves device scalability and can significantly increase speed of production, for example, by avoiding the need for thermal evaporation process that is required for the metal-based electrodes. By utilising the present invention, devices based on printable electrodes can be made with commercially attractive efficiencies and cost.

[0175] The devices in the present invention may be used, for example in PSCs, including perovskite single junction and tandem solar cells.

[0176] The present invention simplifies manufacturing complexity for material preparation (less steps for the material production) and provides a low-cost, low-temperature curable and highly conductive electrode material.

Inclusion of an Interlayer

[0177] A semiconductor device according to the present invention may include an interlayer between the first electrode and the first charge transportation layer. A non-limiting example of a semiconductor device according to the present invention including a graphene interlayer will now be described.

Graphene Interlayer Ink Formation

[0178] Graphene interlayer ink was prepared using the same ink as that used for the counter electrode described previously. In a first step, a fixed amount of the microfluidized graphene ink was dried overnight at 80° C. Afterwards, the as dried graphene nanoplates powder was dispersed in isopropyl alcohol (IPA) at a concentration of 1 mg/ml. Finally, the dispersion was ultrasonicated for ~15 minutes until the graphene nanoplates powder is well dispersed forming a stable ink (see FIG. **12**).

Fabrication of Solar Cells with an Interlayer

[0179] Heterostructure subcells were fabricated based on the procedures described previously up to the step of formation of the P3HT or P3HT:Gr layer (see: Solar cell fabrication). However, following the formation of the P3HT or P3HT:Gr layer, a graphene interlayer thin film was prepared by depositing (spin-coating) the as-prepared ink on top of the P3HT:graphene hybrid HTL film at 3000 rpm. The devices were subsequently completed by doctor blade coating of the microfluidized graphene ink on top of the graphene interlayer. FIGS. **13***a*, **13***b* and **13***c* show the front, back side and a schematic of the front side of the device, respectively.

[0180] The thickness of the wet microfluidized graphene nanoplates film was set to ~0.5 mm, which after the drying process was converted to a ~10 μm thick film. The deposition of the paste was realized in ambient conditions and immediately afterwards, the devices were transferred inside

an oven to dry for approximately half an hour at 80° C. The devices were then left overnight without encapsulation inside a dry box.

Discussion

[0181] The devices were characterized as described previously (see: Characterization of the devices).

[0182] FIG. **14***a* shows a schematic of an example of a device fabricated without an interlayer according to the previously described fabrication method (see: Solar cell fabrication). FIG. **14***b* shows a schematic of an example of a device with a ~10 nm thick interlayer fabricated according to the method described for fabrication of solar cells with an interlayer.

[0183] As can be seen, the present invention including a thin (~10 nm) graphene interlayer film (deposited between the counter electrode and the hole transport layer) has a much thinner (~10 μm thick) graphene counter electrode in comparison with the device fabricated without an interlayer (with a graphene counter electrode thickness of ~25 μm). This may be due to the graphene interlayer film acting as a bridge/scaffold for optimum graphene counter electrode deposition. Devices with the thin graphene interlayer and the ~10 μm thick graphene counter electrode exhibited an enhanced fill factor (>64%) in comparison with devices without an interlayer (63%). PCEs of >13% were achieved for the devices with interlayers and ~10 μm thick graphene counter electrodes (see characteristic I-V curve in FIG. **15**; "Before Post fabrication LiTFSI treatment"), similarly to the devices with a ~25 μm thick graphene counter electrode. The amount of graphene counter electrode ink needed was therefore reduced by a factor of more than 2 by the inclusion of the graphene interlayer film, while the high PCEs were maintained.

[0184] A significant reduction in materials required to produce the graphene counter electrode can therefore be achieved with the present invention by including a thin graphene interlayer film.

Post-Fabrication Treatment

[0185] Further improvements in performance of a semiconductor device according to the present invention may be achieved by a post-fabrication treatment of the device with a metal salt. Without wishing to be bound by theory, such a treatment may result in a significant improvement of an interfacial contact between the first electrode and the first interlayer or the first charge transportation layer. The post-fabrication treatment with metal salt may reduce the presence of gaps between layers of the device.

[0186] Metal salt may be deposited onto the device by solution processing or thermal evaporation.

[0187] It will be understood that depositing salt onto the completed device following device fabrication is not the same as applying salt to each layer of the device during the fabrication process. It will also be understood that a post-fabrication treatment with metal salt may lead to improvements in devices with or without an interlayer.

[0188] The post-fabrication treatment may comprise depositing a solution comprising metal salt onto the first electrode. Without wishing to be bound by theory, the solution may not penetrate the device further than an interface between the first electrode and the first interlayer or the first charge transportation layer.

[0189] In a non-limiting example, a post-fabrication treatment with LiTFSI salt was applied to the solar cells fabricated with an interlayer as previously described (see: Fabrication of solar cells with an interlayer).

[0190] Following the step of being left overnight without encapsulation inside a dry box and after initial I-V characterisation, the devices were placed inside a nitrogen filled glove box and a 20 mM LiTFSI (Sigma-Aldrich) in acetonitrile (ACN) solution was spin casted/infiltrated on top of the graphene counter electrode at 3000 rpm, shown schematically in FIG. **14***c*. Then, the devices were stored again overnight inside a dry box. Finally, the LiTFSI treated devices were measured using exactly the same experimental conditions as before the treatment.

[0191] FIG. **15** shows a comparison of I-V curves obtained for devices before and after the post-fabrication LiTFSI treatment. As can be seen, the efficiency of the devices after the post device fabrication treatment is reproducibly increased by 3% in absolute value, equivalent to 21% enhancement in PCE compared with the PCE before the treatment.

[0192] A summary of various photovoltaic parameters (short circuit current, I_{SC}; open circuit voltage, V_{OC}; FF; PCE) of the different devices prepared and tested in the non-limiting examples described herein is provided in Table 1.

TABLE 1

Summary of photovoltaic parameters of the different devices

Device	I_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	PCE (%)	% ΔPCE
No interlayer	23.00	0.911	63.07	13.21	—
Interlayer	22.46	0.914	64.15	13.17	—
Interlayer + LiTFSI treatment	23.46	0.963	70.44	15.93	+20.9

[0193] All of the photovoltaic parameters were increased in the devices fabricated according to the present invention following the LiTFSI treatment, with I_{SC}, V_{OC} and FF reaching ~23.5 mA/cm^2 (increased by 4.5%), ~0.96V (increased by 5.5%) and ~70.4% (increased by ~10%) respectively (see Table 1) in comparison with the same devices prior to the LiTFSI treatment. The maximum efficiency for a device fabricated according to the present invention of ~16% is one of the highest (if not the highest) ever reported of any monolithic integrated fully printed PSC with HTL.

[0194] FIG. **16***a* shows a comparison of measured photovoltage response vs light intensity for devices before and after the post-fabrication LiTFSI treatment. An increased photovoltage is observed for LiTFSI treated devices across the different light intensities and an improved ideality factor is obtained (~1.6 for LiTFSI treated cells compared with ~2 for untreated cells) for the respective solar cells following the post-fabrication LiTFSI treatment. Without wishing to be bound by theory, this may indicate reduced trap-assisted recombination at the interfaces. In particular, trap-assisted recombination may be reduced at the interface between the perovskite active layer and the first charge transportation layer, and at the interface between the first charge transportation layer and the interlayer and/or the first electrode.

[0195] FIG. **16***b* shows a higher photovoltage and its faster rise for the devices treated with LiTFSI solution. This may indicate faster charge carrier extraction at the respective

selective contacts. FIG. **16***c* shows a slower decay (longer lifetime) of the photovoltage for the LiTFSI treated devices, which may further indicate reduced recombination at the interfaces and increased carrier lifetimes.

[0196] Without wishing to be bound by theory, the reduced recombination at the interfaces and faster charge carrier extraction observed in devices fabricated according to the present invention may be due to improved interfacial contact between the respective layers of the device. For example, the post-fabrication treatment with LiTFSI may reduce the presence of gaps between layers at a given interface.

[0197] Further experiments performed on devices with different interfacial designs show that the post-fabrication LiTFSI treatment is universally applicable for improving the PCE of any fully printable solar cell architecture with printable counter electrodes according to the present invention.

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1. A semiconductor device comprising:

a first electrode comprising conductive material, wherein the conductive material is deposited by ink deposition (for example, layered material inks such as graphene/graphite inks), or wherein the conductive material comprises CVD grown graphene or carbon nanotubes;

a first charge transportation layer, wherein the first charge transportation layer is doped with the conductive material of the first electrode;

an optional first insulation layer;

a perovskite active layer;

an optional second insulation layer;

a second charge transportation layer;

and a second electrode.

2. The semiconductor device according to claim **1**, further comprising an interlayer between the first electrode and the first charge transportation layer.

3. The semiconductor device according to claim **2**, wherein the interlayer comprises a conductive material or an ultrathin (below 5 nm) insulating film; preferably a conductive material.

4. The semiconductor device according to claim **3**, wherein the first electrode and the interlayer comprise the same conductive material.

5. The semiconductor device according to claim **2**, wherein the interlayer has a thickness between 2 nm and 50 nm.

6. The semiconductor device according to any one of claims **2** to **4**, wherein the interlayer is deposited by a printable conductive ink, comprising conductive material(s) and solvent(s).

7. The semiconductor device according to any preceding claim, wherein the first electrode is deposited by a printable conductive ink, comprising conductive material(s) and solvent(s).

8. The semiconductor device according to claim **6** or **7**, wherein the conductive material(s) are layered materials including graphene, graphene/graphite, graphite and MXenes, preferably graphene/graphite, further preferably wherein the conductive material(s) are nanoplates, including graphite/graphene nanoplates.

9. The semiconductor device according to claim **6** or **7**, wherein the conductive material(s) are carbon black, carbon/graphite, graphite and carbon nanotubes.

10. The semiconductor device according to claim **6** or **7**, wherein the conductive material(s) are metal inks, for

example nanowire inks, including silver and copper inks, for example silver and copper nanowire inks.

11. The semiconductor device according to any one of claims **1** to **5**, wherein the first electrode is deposited by CVD and the conductive material is (CVD) grown nanomaterials including graphene or carbon nanotubes.

12. The semiconductor device according to any one of claims **1** to **5**, wherein the first electrode is a first nanoplate electrode, preferably wherein the first nanoplate electrode comprises graphite/graphene nanoplates.

13. The semiconductor device according to any preceding claim, wherein the first charge transportation layer is a semiconducting material, preferably an organic semiconducting material.

14. The semiconductor device according to any preceding claim, wherein the first charge transportation layer is a hole transporting organic semiconducting material selected from the group consisting of PEDOT:PSS, PANI (polyaniline), polypyrrole, optionally substituted, doped poly(ethylene dioxythiophene) (PEDOT);

- Poly(triaryl amines) e.g. PTAA (poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine]);
- copper thiocyanate (CuSCN); benzodithiophene (BDT) based polymer;
- polymer,poly(p-phenylene) PPP; lead phthalocyanine (PbPc); poly(9,9-dioctylfluorene-co-N-(4-(3-methylpropyl))diphenylamine) (TFB); polythiophene (PT); poly(4,4'-bis(N-carbazolyl)-1,1'-biphenyl) (PPN);
- nickel oxide (NiO); copper iodide (CuI); CuInS2 (quantum dots); ternary oxide: $Li_{0.05}Mg_{0.15}Ni_{0.8}O$; or
- small organic molecule HTMs, including spiro OMeTAD; FDT (triazatruxene and others based on the dithiophene core); or PCP-TPA, a triphenyl amine based compound.

15. The semiconductor device according to any preceding claim, wherein the first charge transportation layer is a hole transporting organic semiconducting material selected from the group consisting of polyfluorenes (preferably F8, TFB, PFB or F8-TFB) or Spiro-OMeTAD or polycarbazole (preferably poly(9-vinylcarbazole)) or 4,4'-Bis(N-carbazolyl)-1,1'-biphenyl, or or 4,4'-Bis(N-carbazolyl)-1,1'-biphenyl, or poly(3-hexylthiophene-2,5-diyl) (P3HT) or. poly[(4,4'-bis(2-butyloctoxycarbonyl-[2,2'-bithiophene]-5,5-diyl)-alt-(2,2'-bithiophene-5,5'-diyl) (PDCBT).

16. The semiconductor device according to any preceding claim, wherein the first charge transportation layer is an electron transporting organic semiconducting material selected from the group consisting of poly(fluorene)s, preferably F8, TFB, F8BT or F8-TFB AB copolymer (95:5 F8:TFB);

17. The semiconductor device according to any preceding claim, wherein the first charge transportation layer is doped with 0.5 to 3%, 0.5 to 2.5%, 1 to 3%, 1 to 2%, 0.5, 1, 1.5, 2, 2.5 or 3% of the nanoplate material.

18. The semiconductor device according to any preceding claim, wherein the perovskite is a halide perovskite.

19. The semiconductor device according to any preceding claim, wherein the perovskite is a 3D perovskite, a 2D perovskite, a 1D perovskite and/or a quasi-2D perovskite.

20. The semiconductor device according to any preceding claim, wherein the perovskite is an organic metal halide perovskite or an inorganic metal halide perovskite or a hybrid organic-inorganic metal halide perovskite material.

21. The semiconductor device according to any one of claims **18** to **20**, wherein said metal halide perovskite or metal-metal halide perovskite has an AMX_3 structure, where A is a monovalent cation, M is a divalent cation and X is a halide anion.

22. The semiconductor device according to claim **21**, wherein A may be:

- a monovalent organic cation or a monovalent metal cation;
- dual cationic with an $A_{1-i}B_i$ structure, with A and B being different and are each a monovalent organic cation or monovalent metal cation, and i is between 0 and 1;
- triple cationic with an $A_\alpha B_\beta C_\gamma$ structure, with A, B and C being different and are each a monovalent organic cation or monovalent metal cation, and α, β and γ combined equal 1; or
- quadruple cationic with an $A_\alpha B_\beta C_\gamma D_\delta$ structure, wherein: A, B, C and D are each a monovalent organic cation or monovalent metal cation, where A, B, C and D are different; and α, β, γ and δ combined equal 1.

23. The semiconductor device according to any one of claims **21** to **22**, wherein M may be:

- a divalent cation;
- have the structure $M_{1-j}N_j$ wherein M and N are each a divalent metal cation; and
- j is between 0 and 1; or
- have the structure $M_\epsilon N_\zeta O_\eta$ structure, wherein: M, N and O are each a divalent metal cation, where M, N and O are different; and ϵ, ζ and η combined equal 1.

24. The semiconductor device according to any one of claims **21** to **23**, wherein X_3 may be:

- a halide anion;
- have the structure $X_{3-k}Y_k$, wherein X and Y are each a halide anion, where X and Y are different, and k is between 0 and 3; or
- have the structure $X_\alpha Y_\beta Z_\gamma$ structure, wherein: X, Y and Z are each a halide anion, where A, B and C are different; and α, β and γ combined equal 1.

25. The semiconductor device according to any one of claims **21** to **24**, having the structure selected from:

1	A	M	X_3
2	$A_{1-i}B_i$	M	X_3
3	$A_\alpha B_\beta C_\gamma$	M	X_3
4	A	$M_{1-j}N_j$	X_3
5	$A_{1-i}B_i$	$M_{1-j}N_j$	X_3
6	$A_\alpha B_\beta C_\gamma$	$M_{1-j}N_j$	X_3
7	A	M	$X_{3-k}Y_k$
8	$A_{1-i}B_i$	M	$X_{3-k}Y_k$
9	$A_\alpha B_\beta C_\gamma$	M	$X_{3-k}Y_k$
10	A	$M_{1-j}N_j$	$X_{3-k}Y_k$
11	$A_{1-i}B_i$	$M_{1-j}N_j$	$X_{3-k}Y_k$
12	$A_\alpha B_\beta C_\gamma$	$M_{1-j}N_j$	$X_{3-k}Y_k$
13	A	M	$X_\alpha Y_\beta Z_\gamma$
14	$A_{1-i}B_i$	M	$X_\alpha Y_\beta Z_\gamma$
15	$A_\alpha B_\beta C_\gamma$	M	$X_\alpha Y_\beta Z_\gamma$
16	A	$M_{1-j}N_j$	$X_\alpha Y_\beta Z_\gamma$
17	$A_{1-i}B_i$	$M_{1-j}N_j$	$X_\alpha Y_\beta Z_\gamma$
18	$A_\alpha B_\beta C_\gamma$	$M_{1-j}N_j$	$X_\alpha Y_\beta Z_\gamma$

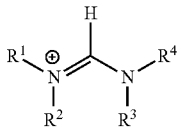
26. The semiconductor device according to any one of claims **21** to **25**, wherein the monovalent cation(s) is/are an alkali metal cation.

27. The semiconductor device according to claim **26**, wherein the alkali metal cation(s) is/are selected from caesium (Cs^+), rubidium (Rb^+) and/or potassium (K^+).

28. The semiconductor device according to any one of claims **21** to **27**, wherein the monovalent cation(s) is/are a

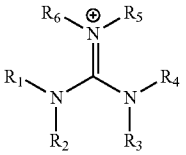
primary, secondary or tertiary ammonium cation $[HNR^1R^2R^3]^+$, wherein each of R^1, R^2 and R^3 is the same or is different and is selected from hydrogen, an unsubstituted or substituted C_1-C_{20} alkyl group and an unsubstituted or substituted C_5-C_{18} aryl group.

29. The semiconductor device according to any one of claims **21** to **28**, wherein the monovalent cation(s) is/are of the form $[R^1R^2N{-}CH{=}NR^3R^4]^+$:



wherein each of R^1, R^2, R^3 and R^4 is the same or is different and is selected from hydrogen, an unsubstituted or substituted C_1-C_{20} alkyl group and an unsubstituted or substituted C_5-C_{18} aryl group.

30. The semiconductor device according to any one of claims **21** to **29**, wherein the monovalent cation(s) is/are of the form $(R^1R^2N)(R^3R^4N)C{=}NR^5R^6$:



wherein each of R^1 R^2, R^3, R^4, R^5 and R^6 is the same or is different and is selected from hydrogen, an unsubstituted or substituted C_1-C_{20} alkyl group and an unsubstituted or substituted C_5-C_{18} aryl group.

31. The semiconductor device according to any one of claims **21** to **30**, wherein the divalent cation M is a divalent metal cation.

32. The semiconductor device according to claim **31**, wherein the divalent metal cation(s) is tin (Sn^{2+}), lead (Pb^{2+}), cobolt (Co^{2+}) and/or zinc (Zn^{2+}).

33. The semiconductor device according to any one of claims **27** to **32**, wherein X is a halide anion(s) selected from one or more of chloride, bromide, iodide, and fluoride and, in the AMX_3 structure each halide is the same or is different.

34. The semiconductor device according to claim **33**, wherein the halide ion is or includes bromide.

35. The semiconductor device according to any preceding claim, wherein the second charge transportation layer is a semiconducting material, preferably an organic semiconducting material.

36. The semiconductor device according to any preceding claim, wherein the second charge transportation layer is an electron transport materials (ETLs) including inorganic ETLs like TiO_2; ZnO; SnO_2; ZrO_2; $SrTiO_3$; $ZnSnO_4$; or WO_3 or organic ETLs like PCBM:polystyrene; PCBM: PMMA C60; PEHT; or polyethyleneimine (PEI); PCBM.

37. The semiconductor device according to claim **35**, wherein the second charge transportation layer is an electron transporting inorganic semiconducting material selected from the group consisting of titanium dioxide (TiO_2), zinc oxide (ZnO), magnesium zinc oxide (MgZnO) and aluminium-doped ZnO (AZO); or metal oxide hot transporters, for example NiO.

38. The semiconductor device according to any preceding claim, wherein the second electrode is formed of a transparent conductive material.

39. The semiconductor device according to claim **38**, wherein the second electrode is selected from: indium tin oxide (ITO), fluorine doped tin oxide (FTO), indium zinc oxide, graphene, carbon nanotubes, silver nanowires, and/or a metal with a thickness of up to 100-150 nm thick.

40. The semiconductor device according to any preceding claim comprising a first insulation layer.

41. The semiconductor device according to any preceding comprising a second insulation layer.

42. The semiconductor device according to any preceding claim wherein the insulation layer(s) is/are formed of an wherein the insulating layer is formed of an insulating polymer and is optionally selected from the group consisting of poly(ethyleneimine) (PEI), polyethylenimine-ethoxylated (PEIE), polystyrene (PS), poly(methylmethacrylate) (PMMA), phenethylammonium iodide (PEAI), Guanidinium iodide (GuI) Guanidinium bromide (GuBr), n-Butylamonium iodide (BAI), n-Butylammonium bromide (n-BABr) and ethylenediammonium diiodide ($EDAI_2$).

43. The semiconductor device according to any preceding claim wherein the insulation layer(s) is/are formed of an oxide or nitride, optionally selected from the group consisting of aluminium oxide, silicon dioxide, silicon nitride, zinc oxide modified with aluminium oxide, nickel oxide, fluorine-containing insulating polymers, poly(perfluorobutenylvinylether) (Cytop) or magnesium oxide.

44. The semiconductor device according to any preceding claim wherein the insulation layer(s) have a thickness of less than 30 nm.

45. The semiconductor device according to any preceding claim, wherein the insulating layer(s) is/are deposited by atomic layer deposition (ALD), spin coating or thermal evaporation.

46. The semiconductor device according to any preceding claim, wherein one or more metal salt(s) with electron accepting (p-type doping) properties is present at one or more interfaces between layers of the semiconductor device.

47. The semiconductor device according to any preceding claim, wherein one or more metal salt(s) with electron accepting (p-type doping) properties is present at an interface between the first charge transportation layer and a layer of the semiconductor device adjacent the first charge transportation layer.

48. The semiconductor device according to any preceding claim, wherein one or more metal salt(s) with electron accepting (p-type doping) properties is present at an interface between the first electrode and a layer of the semiconductor device adjacent the first electrode.

49. The semiconductor device according to any preceding claim, wherein one or more metal salt(s) with electron accepting (p-type doping) properties is present at an interface between the first electrode and the first interlayer or the first charge transportation layer.

50. The semiconductor device according to any one of claims **46** to **49**, wherein said metal salt(s) is operable to improve an interfacial contact between layers of the semiconductor device.

51. The semiconductor device according to any one of claims **46** to **49**, wherein said metal salt(s) is a lithium metal salt; said lithium metal salt(s) optionally being selected from bis(trifluoromethane)sulfonimide lithium (LiTFSI) salt.

52. The semiconductor device according to any one of claims **46** to **49**, wherein said metal salt(s) is a cobalt metal salt; said cobalt metal salt(s) optionally being selected from tris(2-(1H-pyrazol-1-yl)pyridine)cobalt(III) (FK102), tris(2-(1H-pyrazol-1-yl)-4-tert-butylpyridine)cobalt(III) tri [hexafluorophosphate] (FK209) and bis(2,6-di(1H-pyrazol-1-yl)pyridine)cobalt(III)tris(bis(trifluoromethylsulfonyl) imide) (FK269), tris[2-(1H-pyrazol-1yl)pyrimidine]cobalt (II I) tri[bis(trifluoromethylsulfonyl)imide] (MY11), and bipyridine cobalt complexes.

53. The semiconductor device according to any one of claims **46** to **49**, wherein said metal salt(s) is a copper metal salt; said copper metal salt(s) optionally being selected from CuI, CuSCN, copper(II)-pyridine complexes including bis [di(pyridin-2-yl)methane] copper(II) bis[bis(trifluoromethyl-sulfonyl) imide][Cu(bpm)$_2$] and bis[2,2'-(chloromethylene)-dipyridine] copper(II) bis[bis (trifluoromethylsulfonyl) imide][Cu(bpcm)$_2$], and Cu(bpcm)$_2$.

54. The semiconductor device according to any one of claims **46** to **49**, wherein said metal salt(s) is a silver metal salt; said silver metal salt(s) optionally being selected from AgTFSI.

55. The semiconductor device according to any one of claims **46** to **49**, wherein said metal salt(s) is an iron metal salt; said iron metal salt(s) optionally being selected from $FeCl_3$.

56. The semiconductor device according to claim **46**, wherein said metal salt(s) is bis(trifluoromethane)sulfonimide lithium (LiTFSI) salt.

57. A semiconductor device comprising: a first nanoplate electrode; a first charge transportation layer, wherein the first charge transportation layer is doped with nanoplate material; an insulation layer; and a perovskite active layer.

58. A method of making a semiconductor device comprising a first electrode, a charge transportation layer and a perovskite active layer, the method comprising forming the first electrode by applying a printable conductive ink comprising a conductive material dispersed in a solvent to the device, wherein the solvent is selected to be compatible with the perovskite layer and is selected from IPA, ethanol or ethyl acetate.

59. A method of making a semiconductor device comprising a first electrode made from a chargeable material and an adjacent charge transportation layer, the method comprising doping the adjacent charge transportation layer with the same chargeable material in the first electrode.

60. The method according to claim **58** or **59**, wherein the first electrode comprises a nanoplate material and the charge transportation is doped with said nanoplate material.

61. The method according to any one of claims **58** to **60**, further comprising applying one or more metal salt(s) as defined in any one of claims **49** to **56** to the surface of the first electrode.

62. The method of making a semiconductor device according to any one of claims **58** to **61**, further comprising depositing a solution comprising one or more metal salt(s) as defined in any one of claims **49** to **56** onto the first electrode.

63. The method according to any one of claims **58** to **62**, wherein the semiconductor device has the features of claims **1** to **57**.

64. A method of forming a semiconductor device according to any one of claims **1** to **57**.

65. A solar cell comprising a semiconductor device according to any one of claims **1** to **57** or a semiconductor device manufactured according to any one of claims **58** to **64**.

66. A light emitting device comprising a semiconductor device according to any one of claims **1** to **57** or a semiconductor device manufactured according to any one of claims **58** to **64**.

67. A semiconductor device substantially as hereinbefore described with reference to the accompanying examples.

68. A method for forming a semiconductor device substantially as hereinbefore described with reference to the accompanying examples.

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